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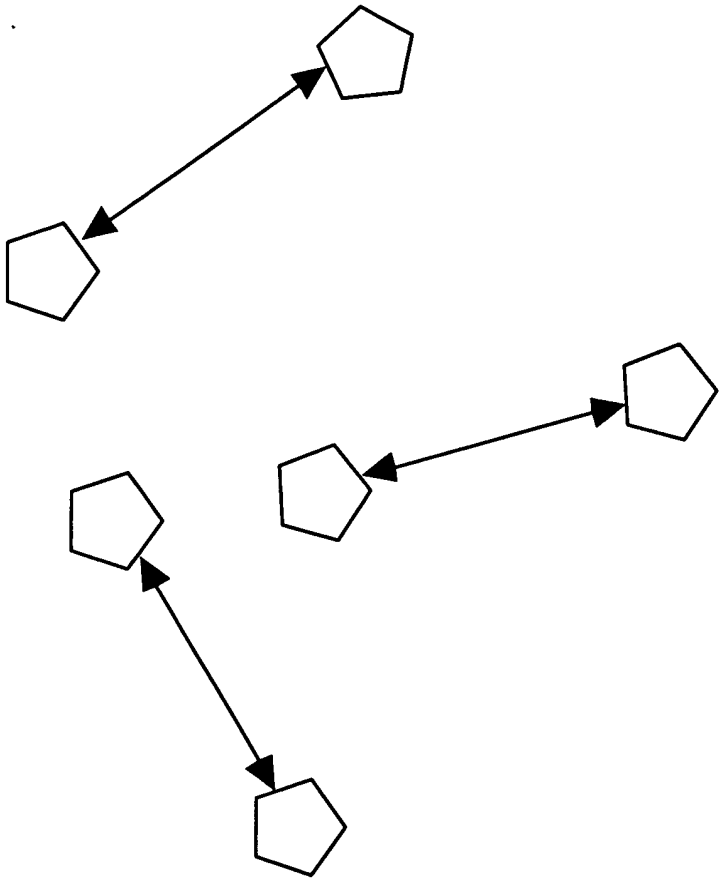

FIG. 1
Prior Art

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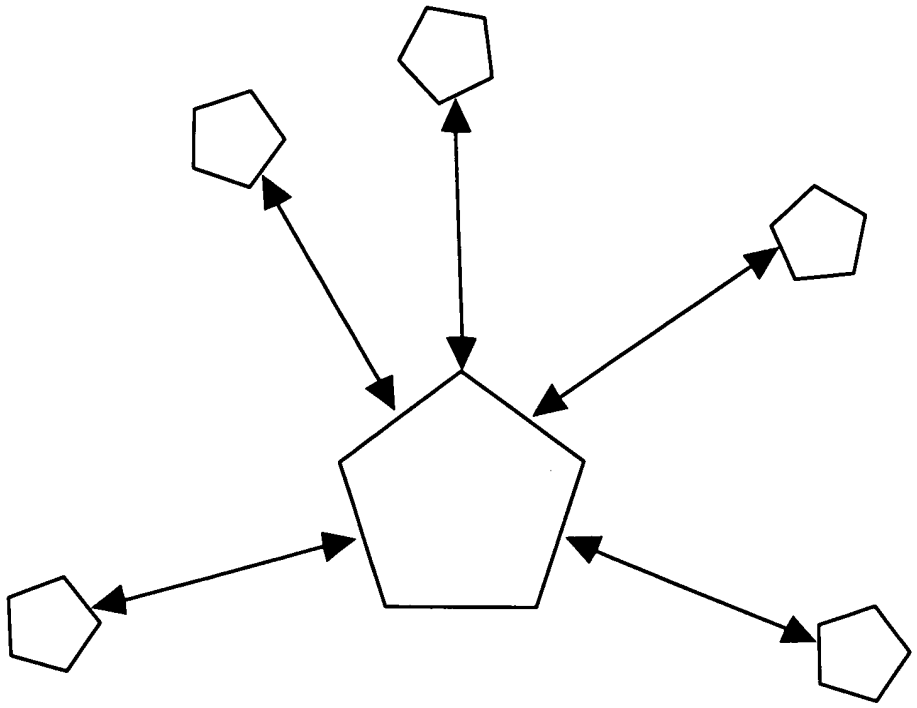

FIG. 2
Prior Art

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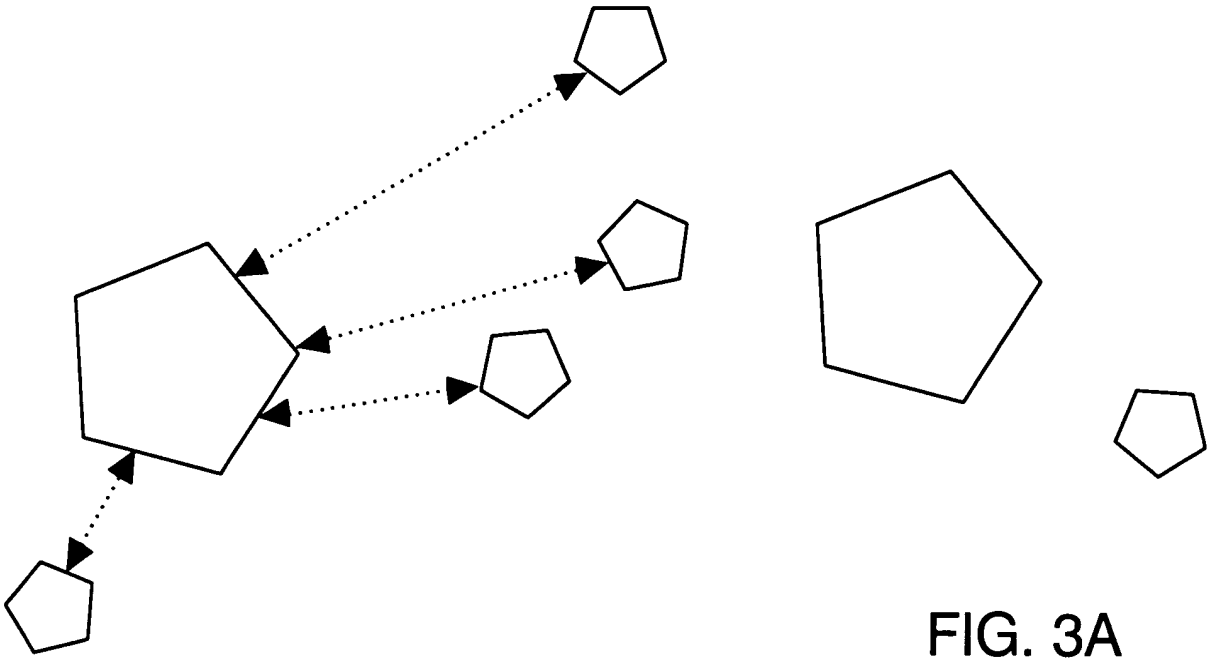

FIG. 3A
Prior Art

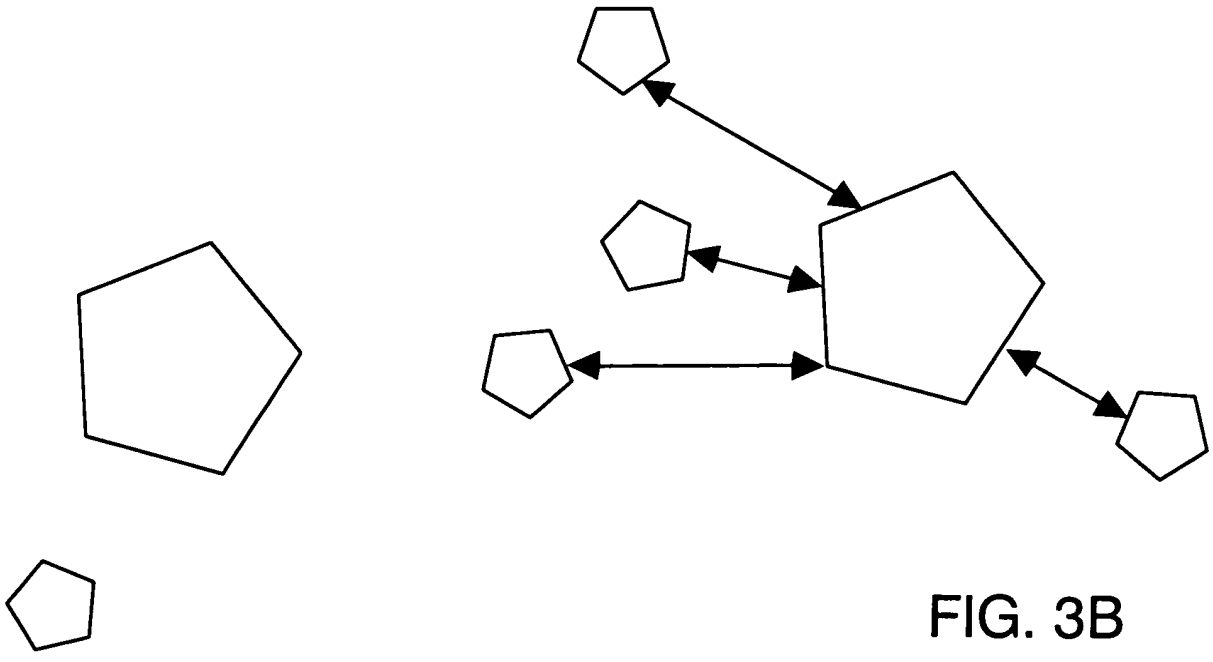

FIG. 3B
Prior Art

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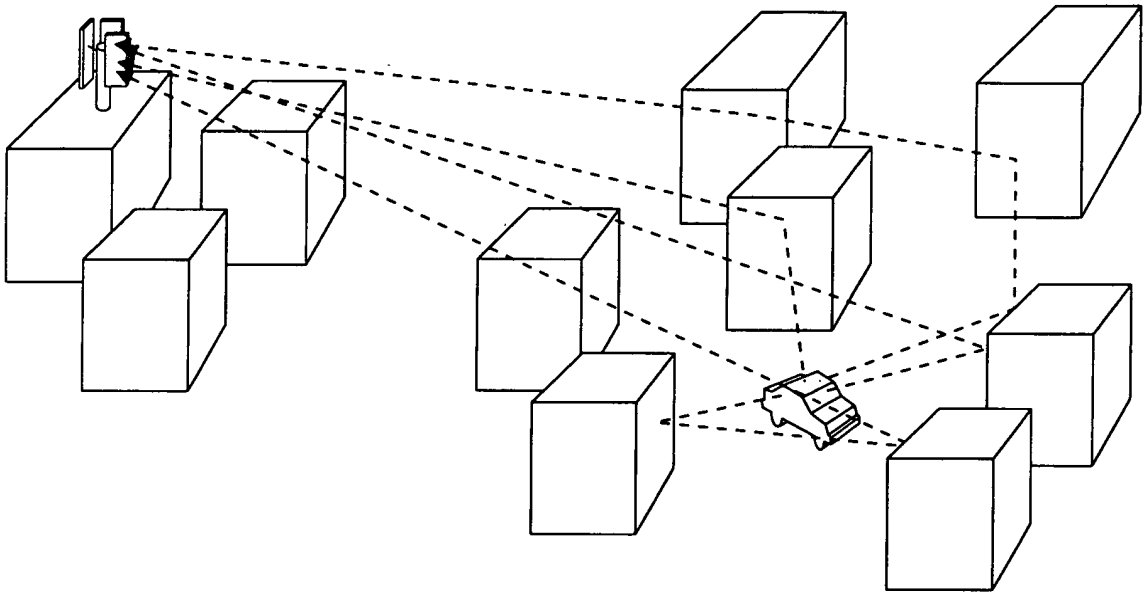

FIG. 4
Prior Art

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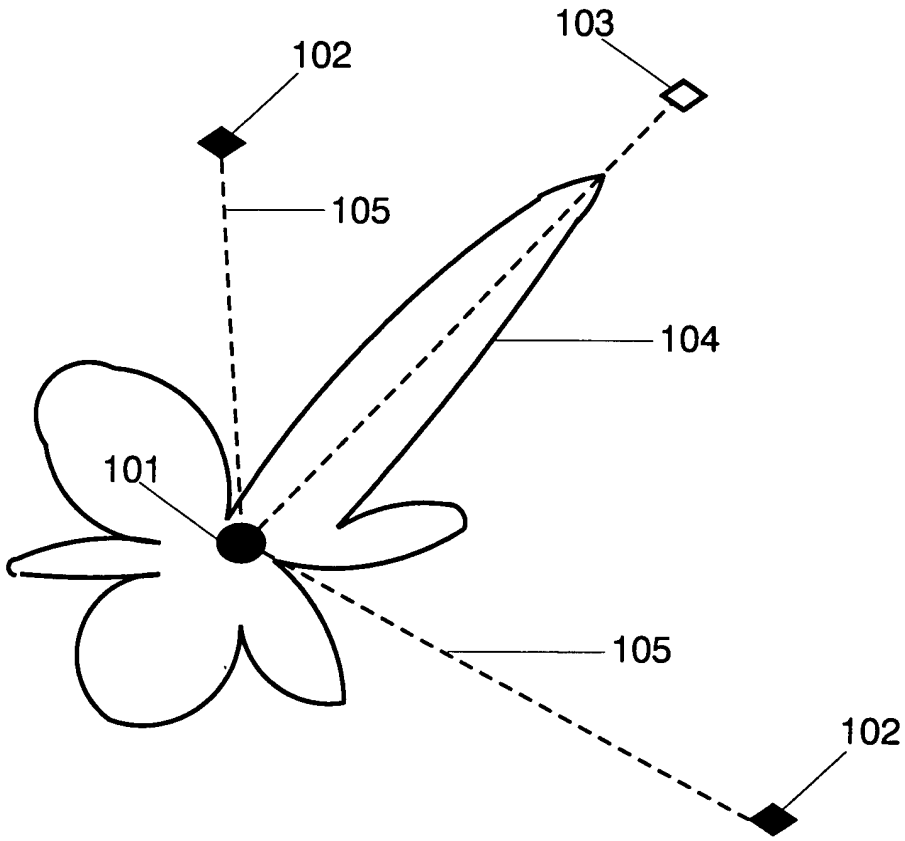

FIG. 5
Prior Art

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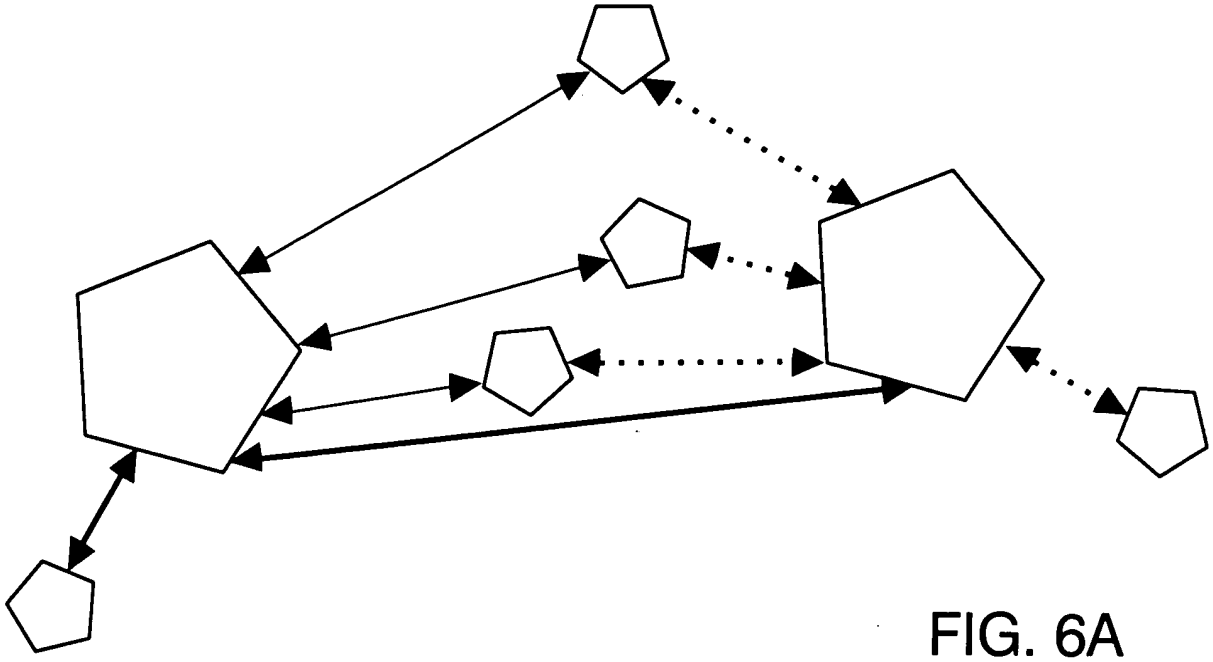

FIG. 6A
Prior Art

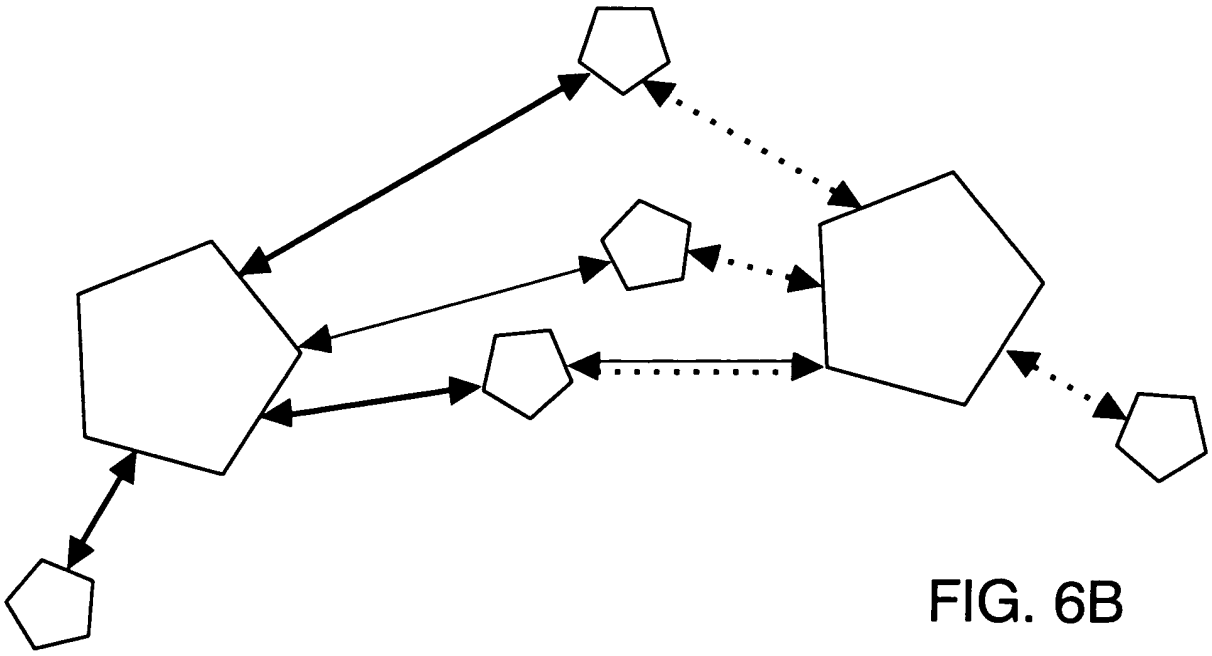

FIG. 6B

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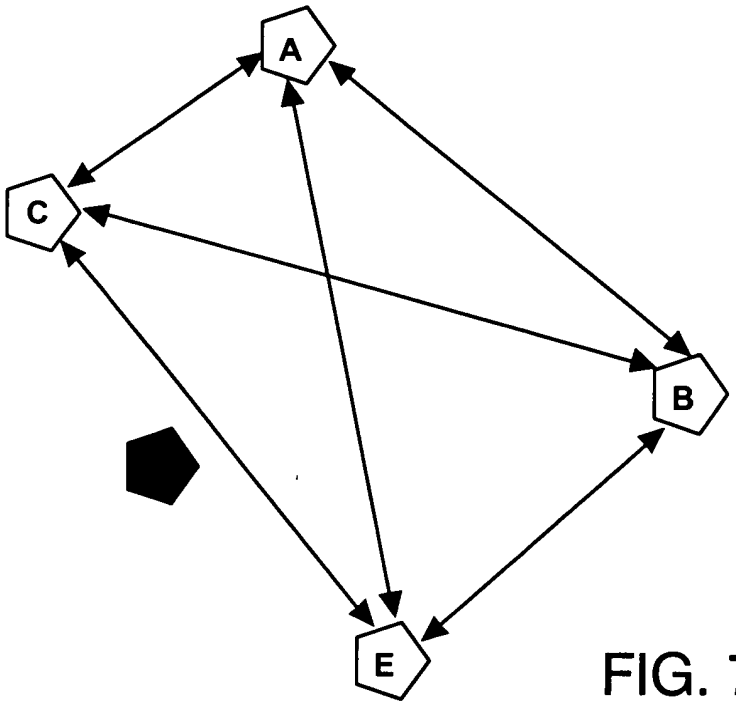

FIG. 7A
Prior Art

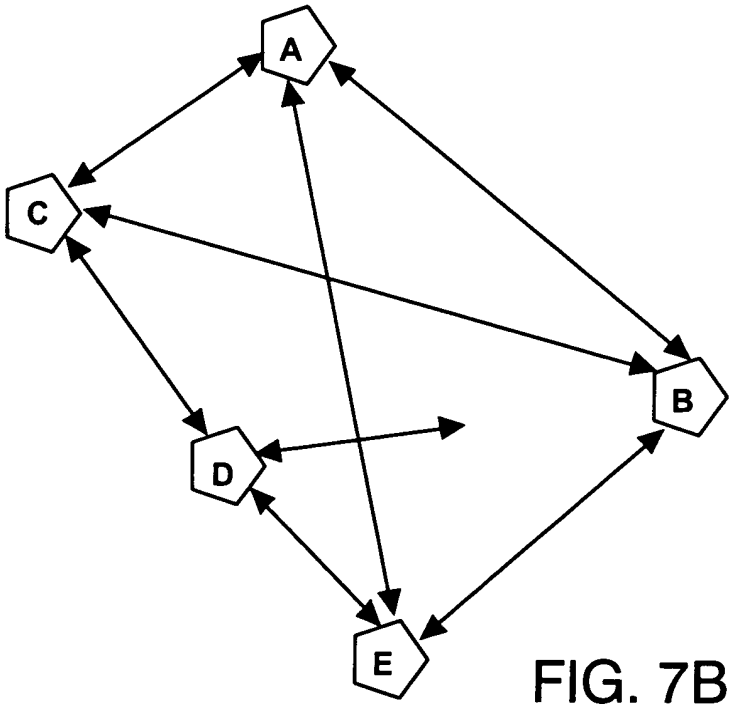

FIG. 7B
Prior Art

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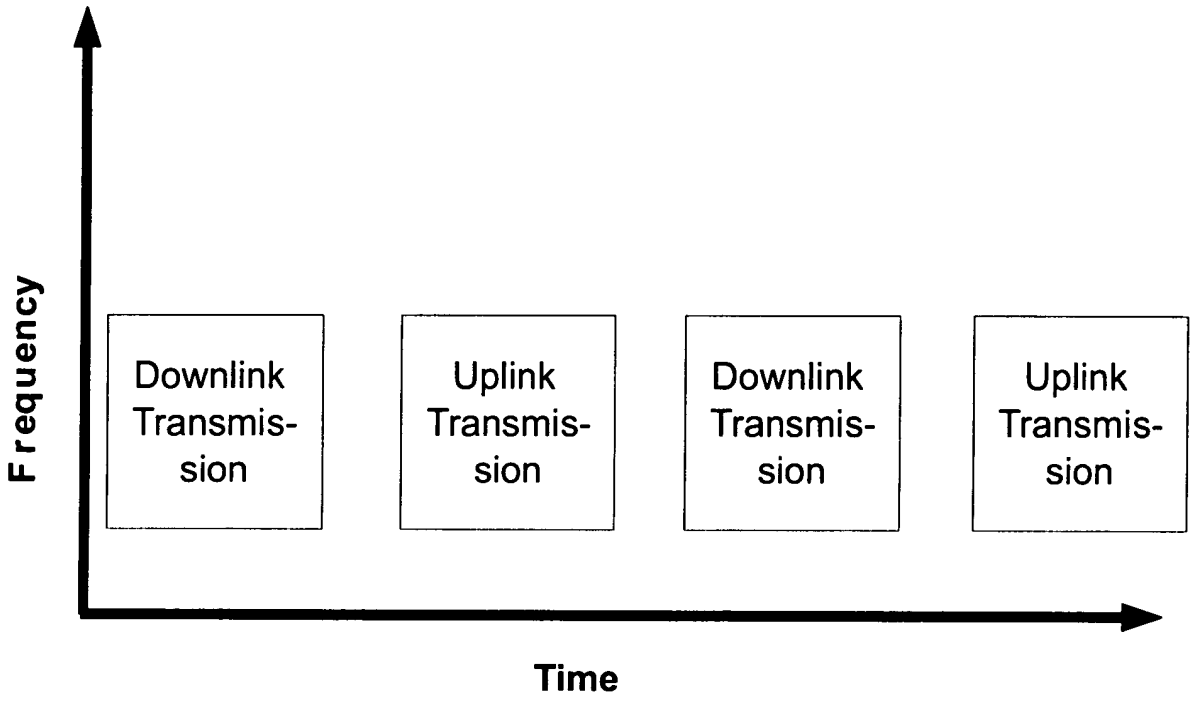

FIG. 8
Prior Art

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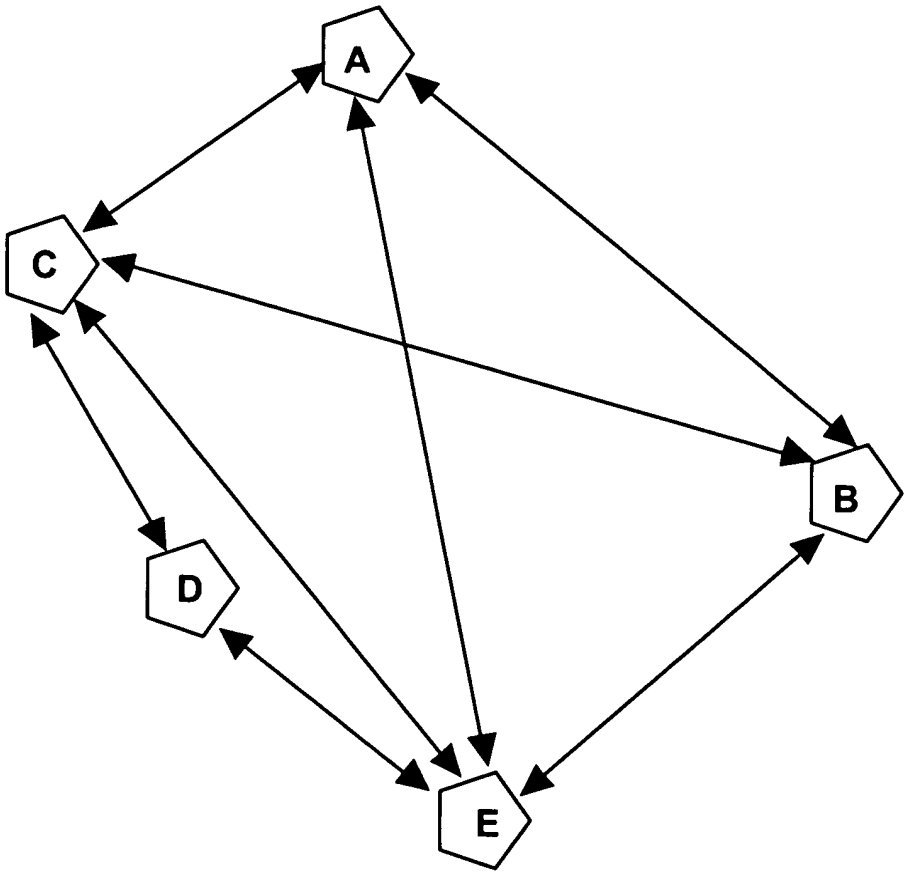

FIG. 9
Prior Art

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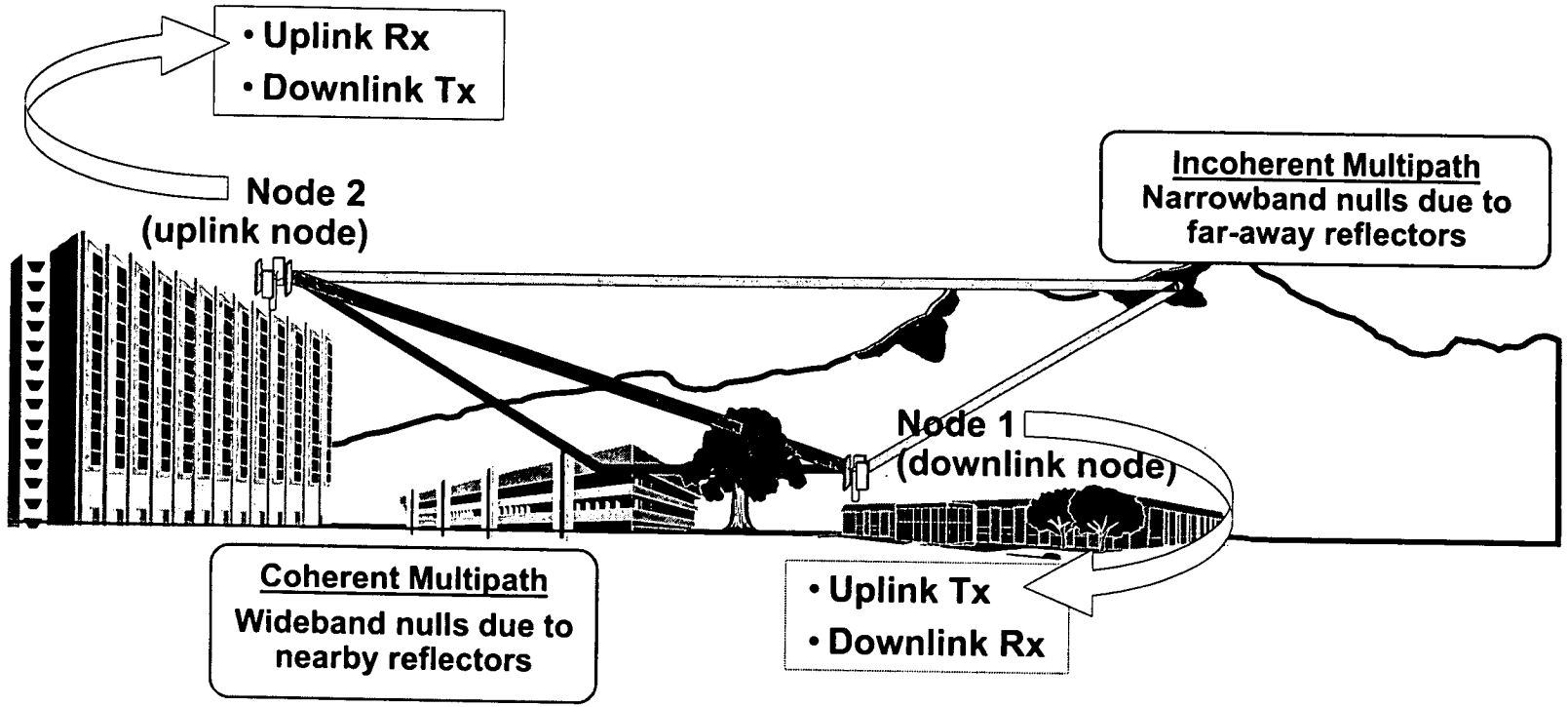

FIG. 10
Prior Art

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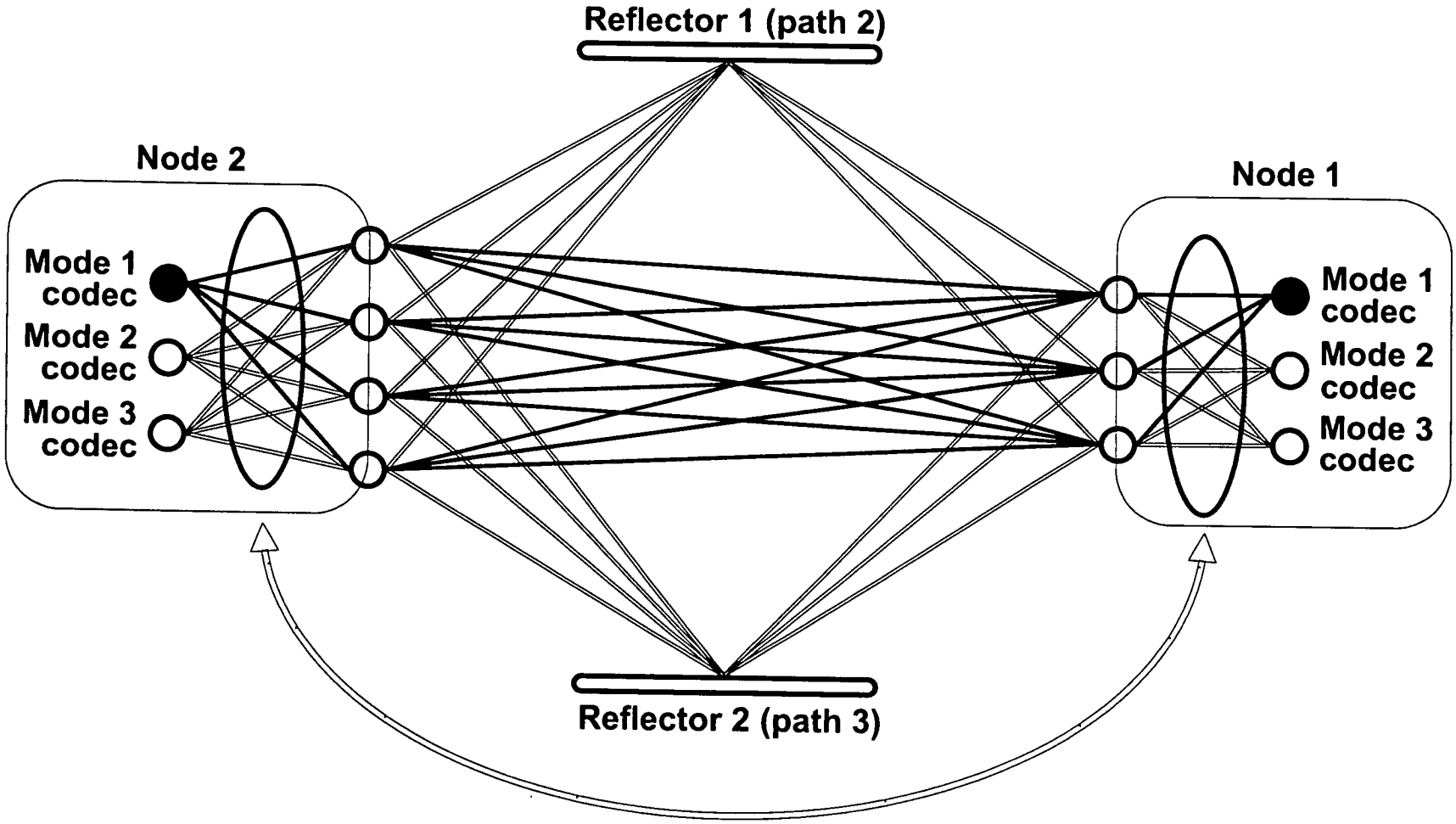

FIG. 11
Prior Art

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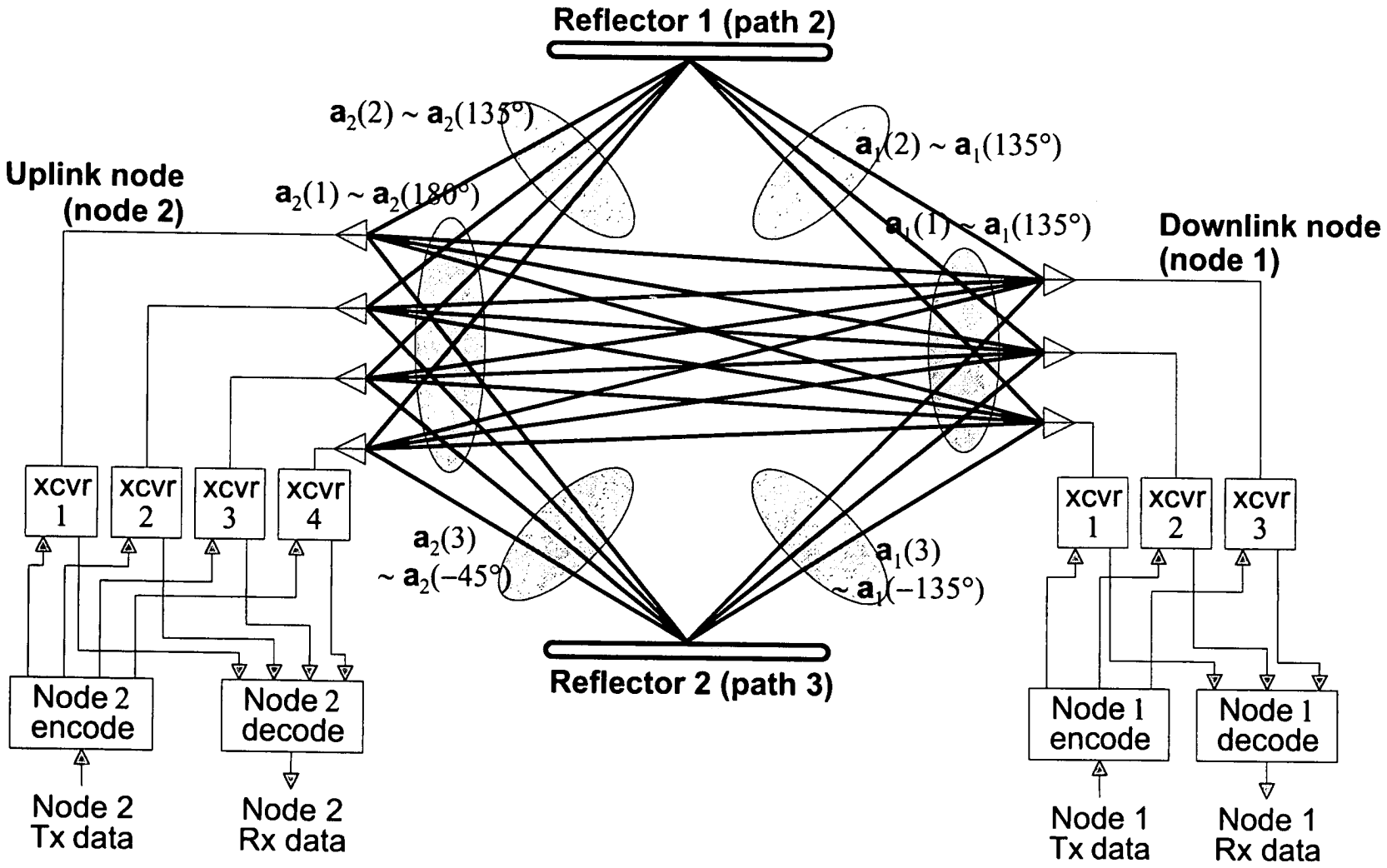

FIG. 12
Prior Art

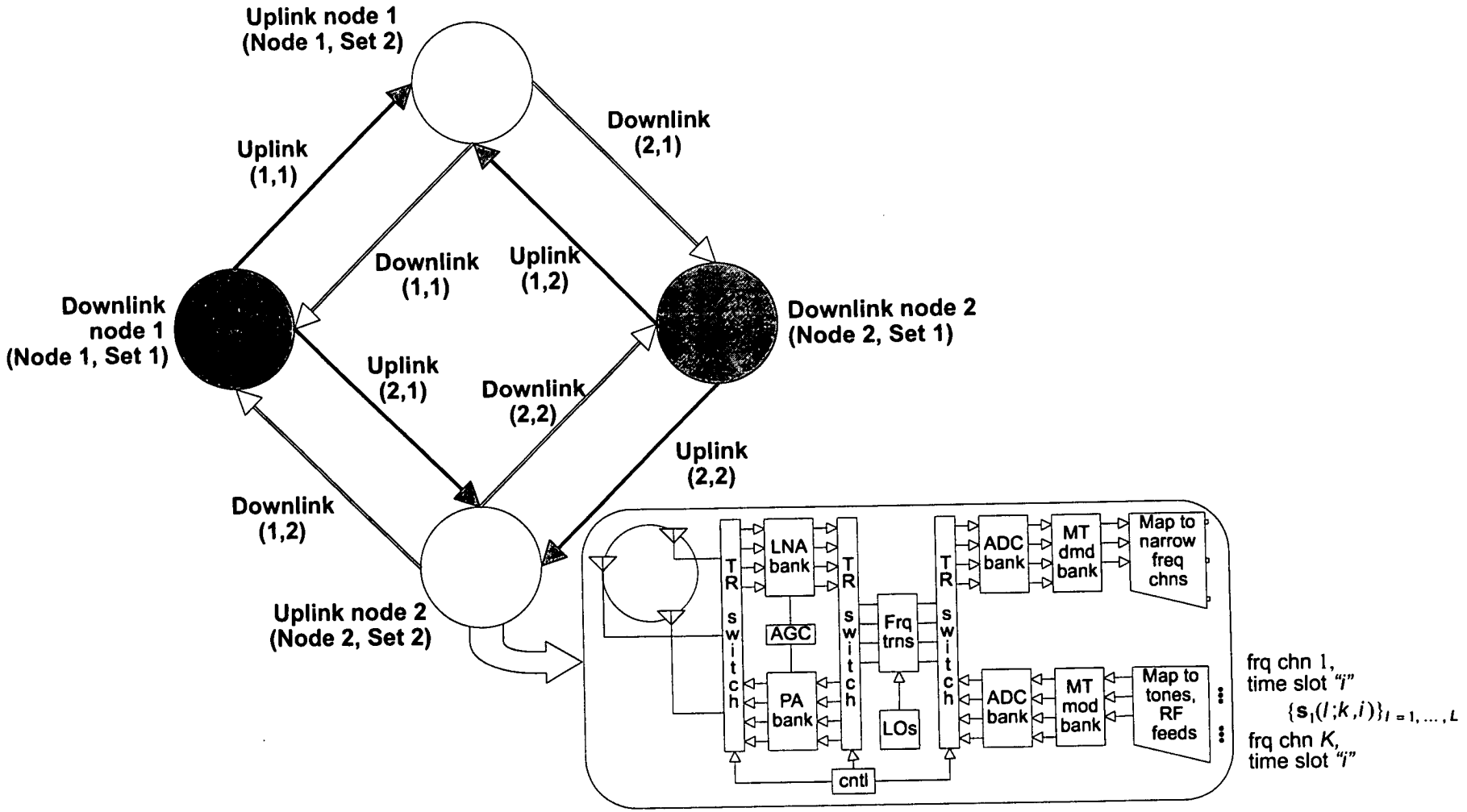
Uplink node 1
(Node 1, Set 2)
Uplink
(1,1)
Downlink
(2,1)
Downlink
(1,1)
Uplink
(1,2)
Downlink
node 1
(Node 1, Set 1)
Downlink node 2
(Node 2, Set 1)
Uplink
(2,1)
Downlink
(2,2)
Uplink
(2,2)
Downlink
(1,2)
Uplink node 2
(Node 2, Set 2)
TR switch
LNA bank
AGC
PA bank
TR switch
Frq trns
LOs
TR switch
ADC bank
MT dmd bank
Map to narrow freq chns
ADC bank
MT mod bank
Map to tones, RF feeds
cntl
frq chn 1,
time slot "i"
$\{s_1(l;k,i)\}_{l=1,\ldots,L}$
frq chn K,
time slot "i"

FIG. 13

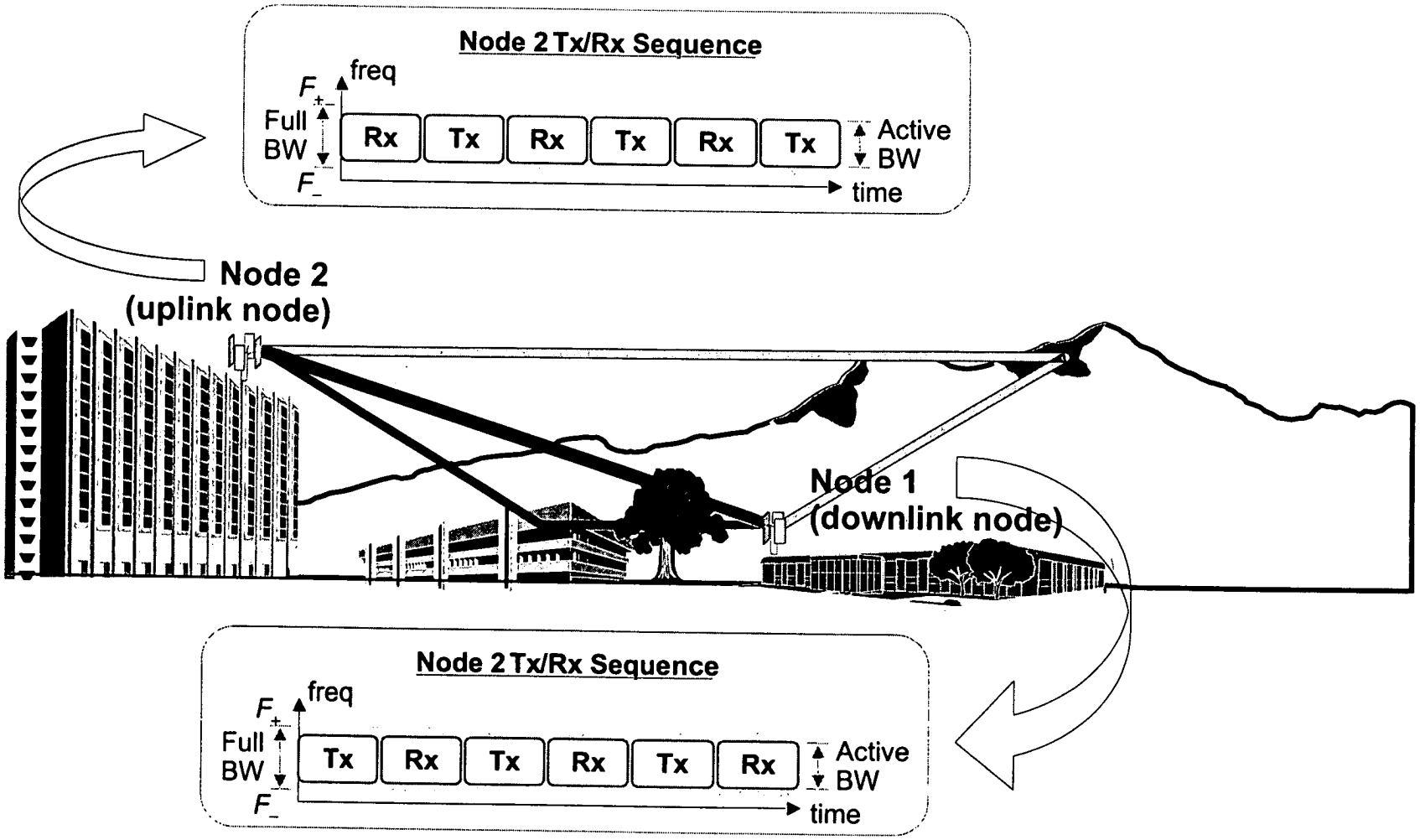

FIG. 14
Prior Art

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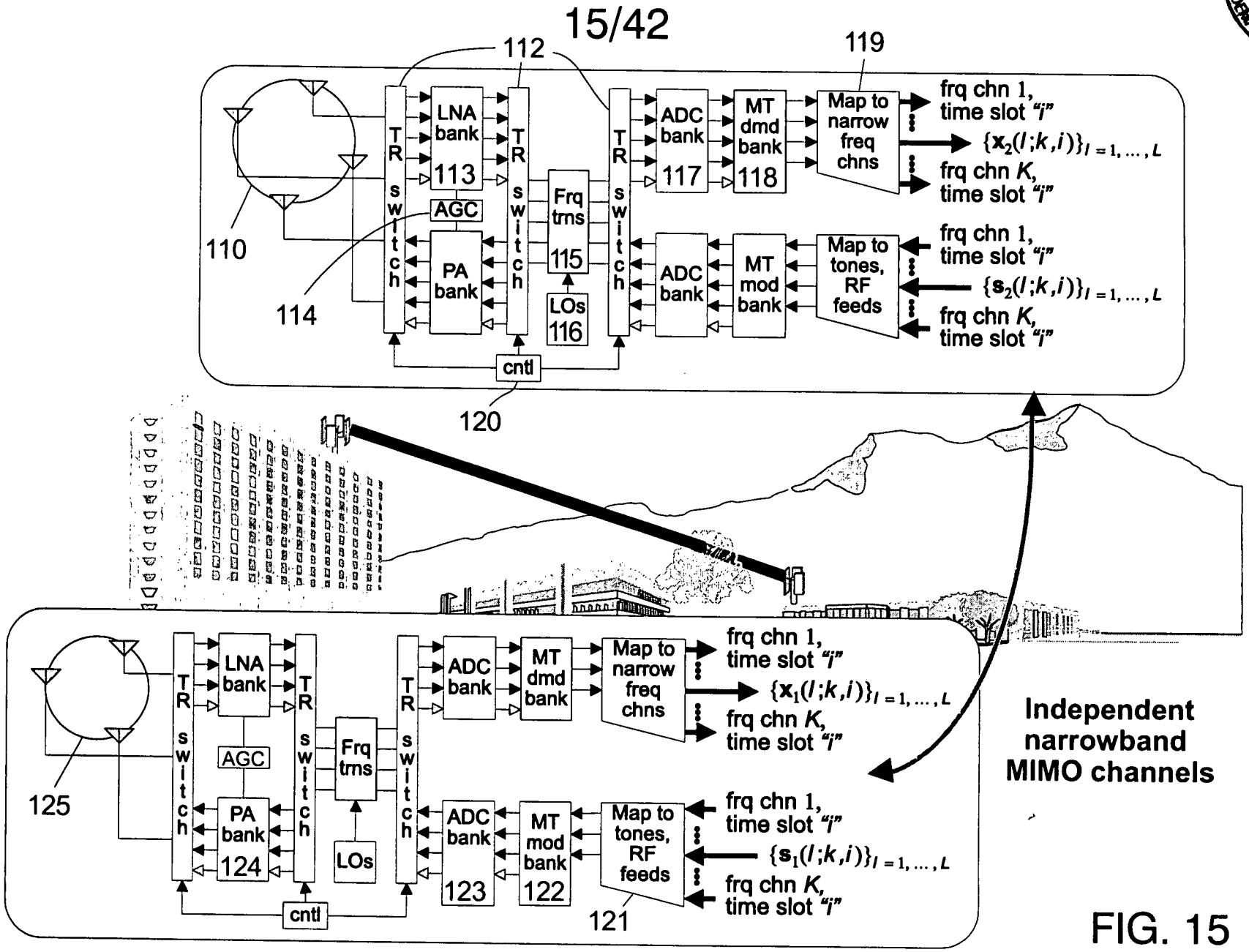

FIG. 15

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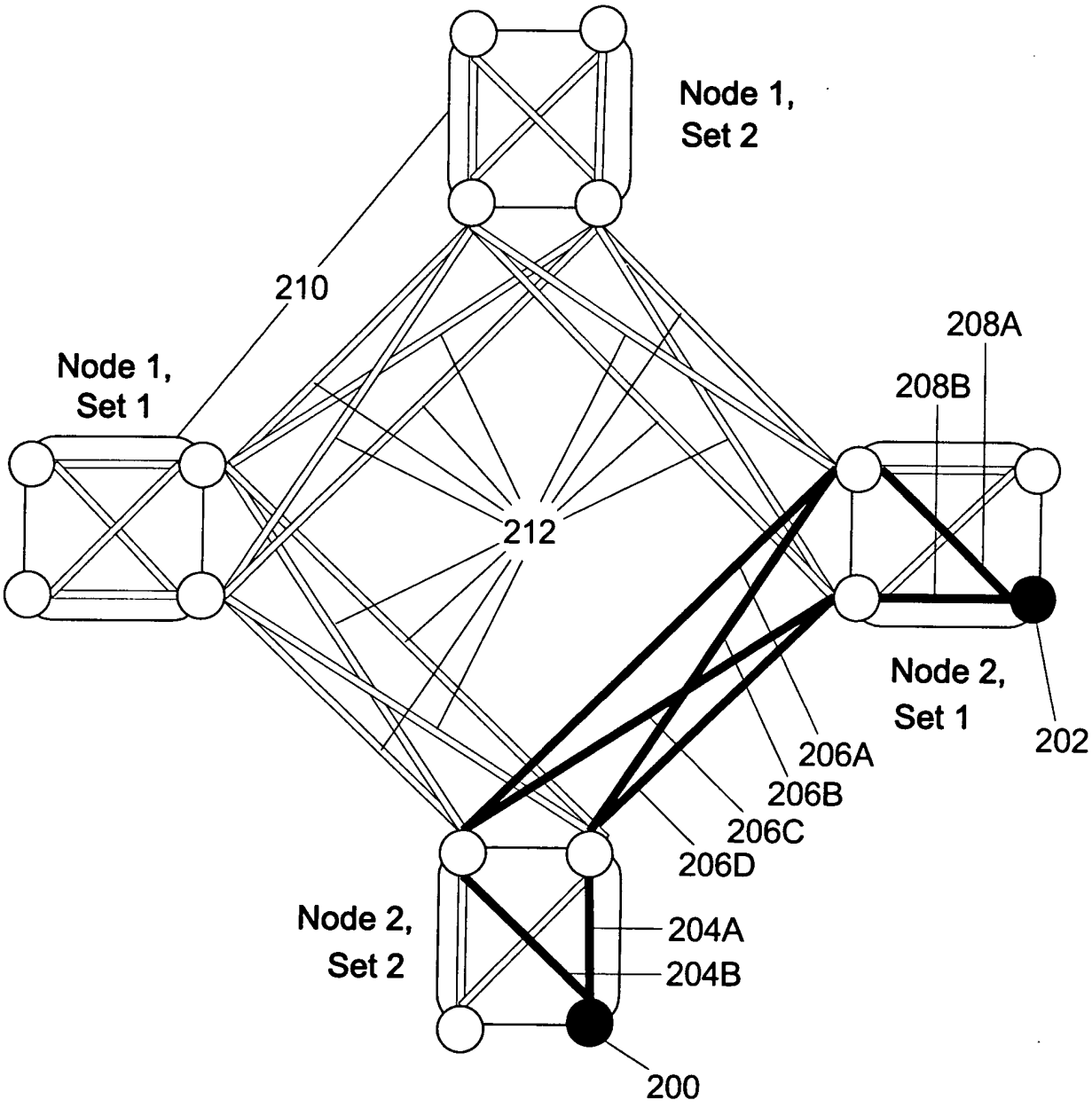

FIG. 16

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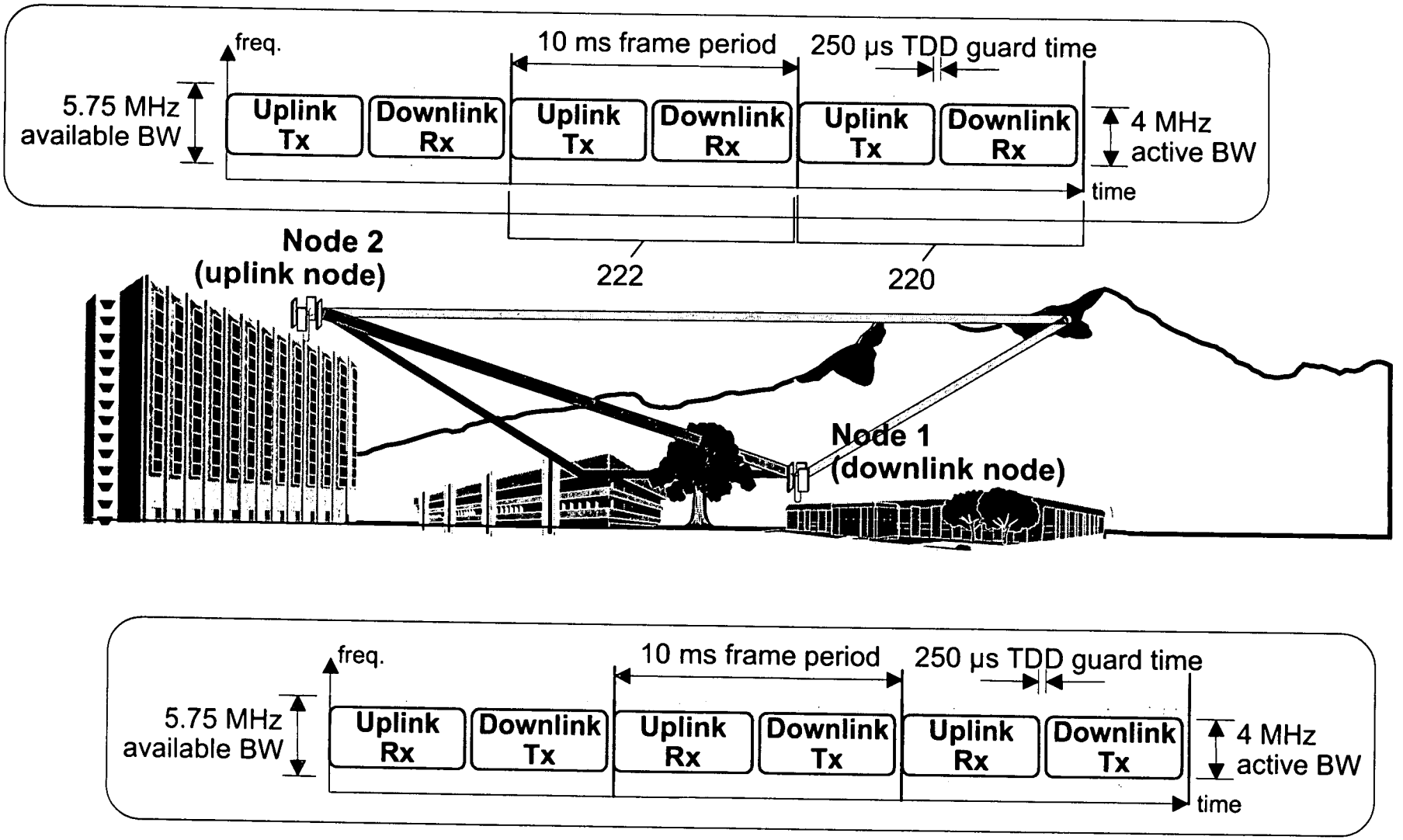

FIG. 17

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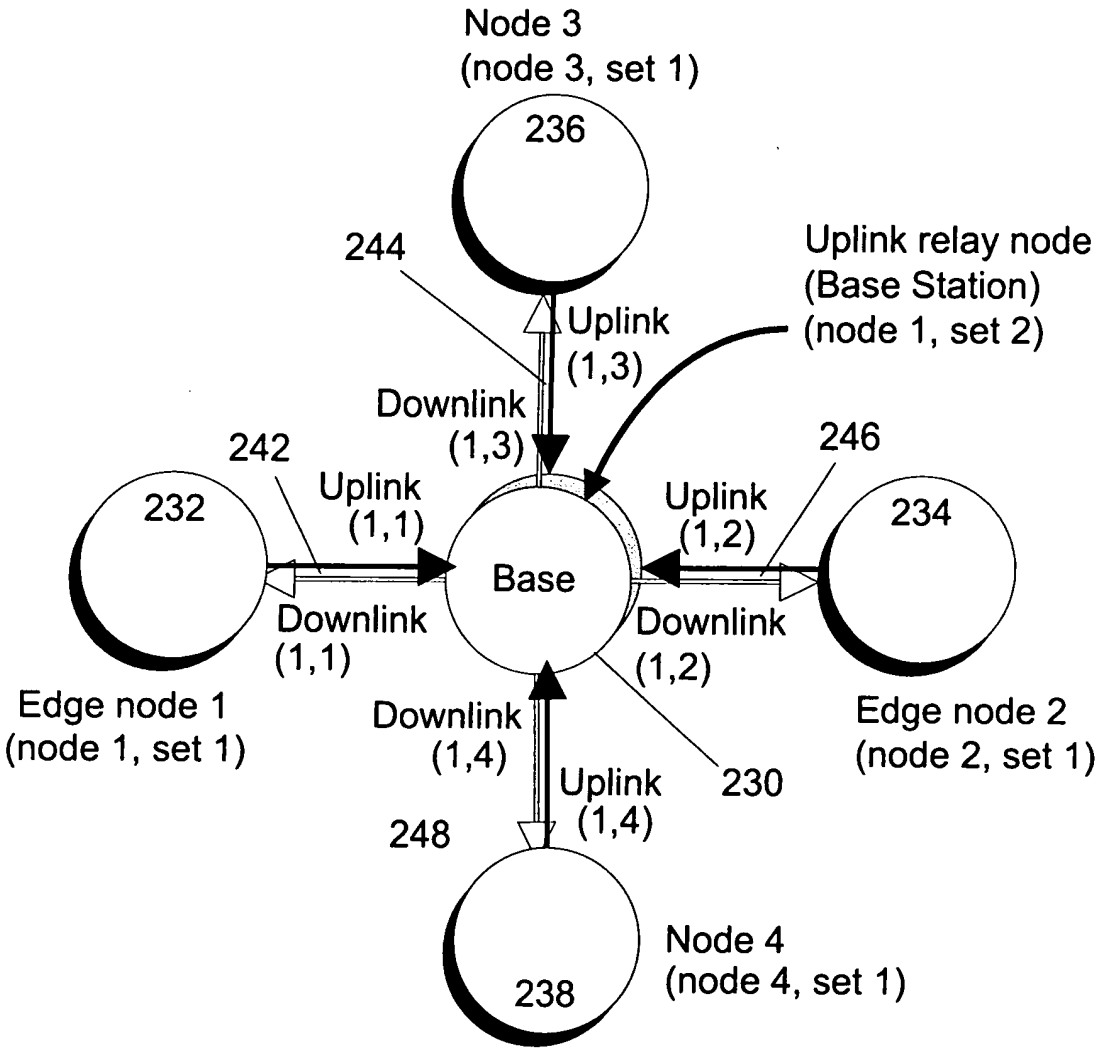

FIG. 18

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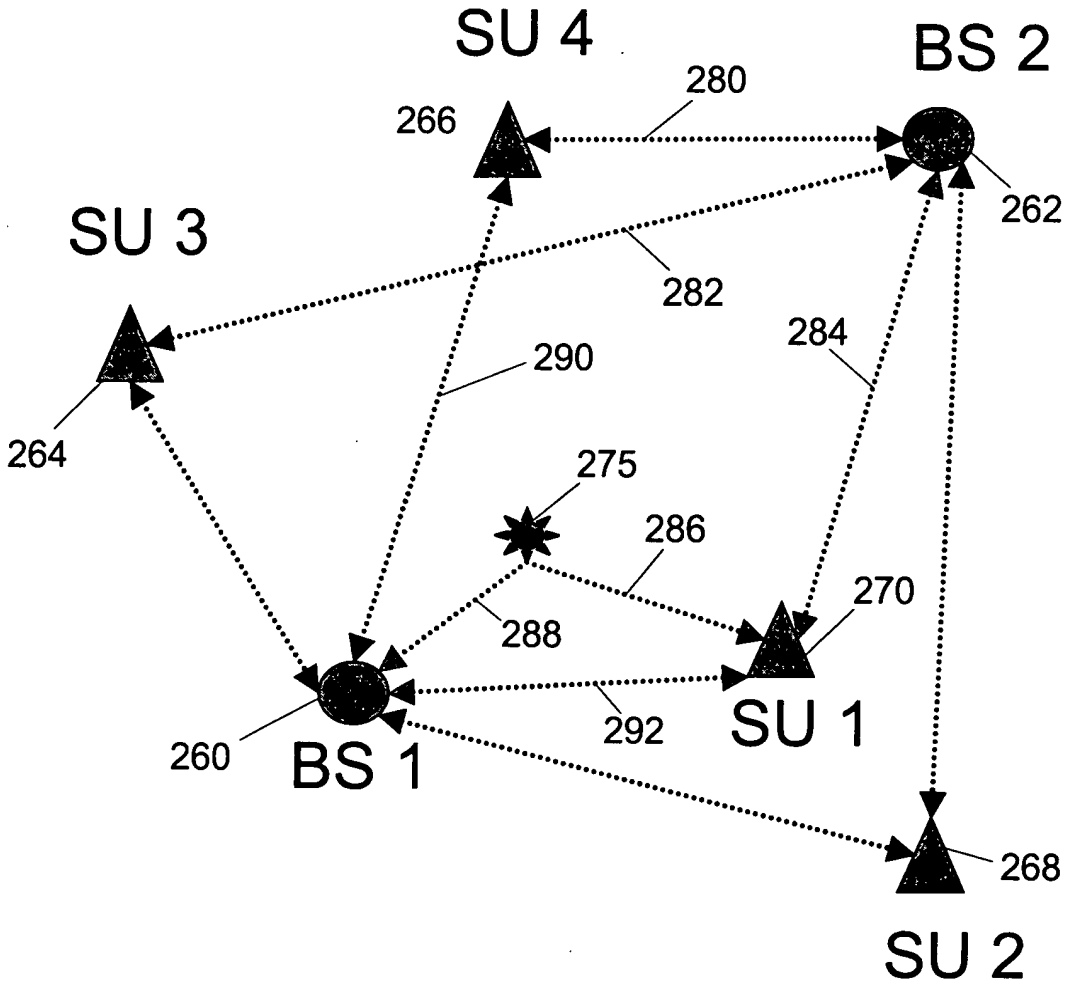
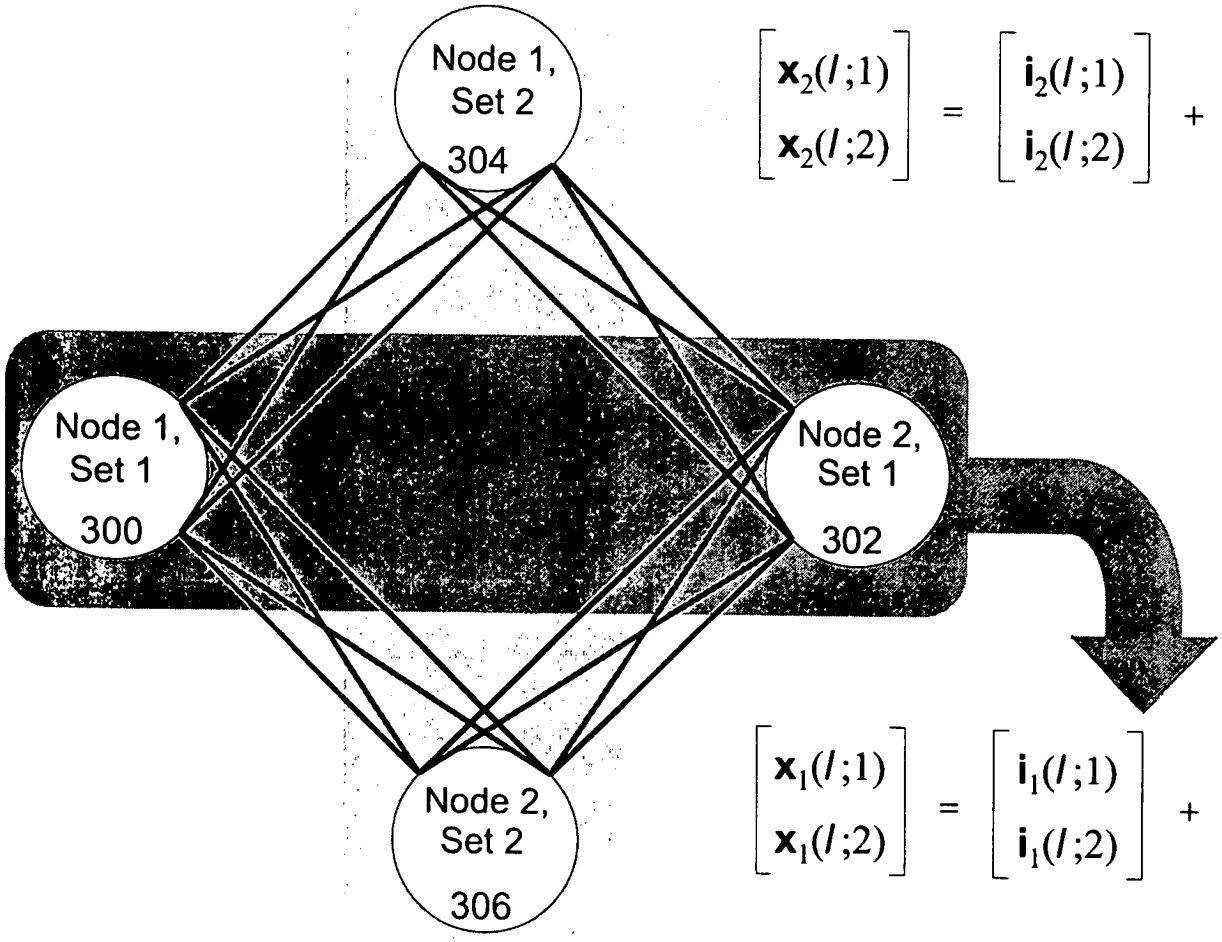


FIG. 19



$$\begin{bmatrix} \mathbf{x}_2(l;1) \\ \mathbf{x}_2(l;2) \end{bmatrix} = \begin{bmatrix} \mathbf{i}_2(l;1) \\ \mathbf{i}_2(l;2) \end{bmatrix} + \begin{bmatrix} \mathbf{H}_{21}(l;1,1) & \mathbf{H}_{21}(l;1,2) \\ \mathbf{H}_{21}(l;2,1) & \mathbf{H}_{21}(l;2,2) \end{bmatrix} \begin{bmatrix} \mathbf{s}_1(l;1) \\ \mathbf{s}_1(l;2) \end{bmatrix}$$

Reciprocal at network level

$$\begin{bmatrix} \mathbf{x}_1(l;1) \\ \mathbf{x}_1(l;2) \end{bmatrix} = \begin{bmatrix} \mathbf{i}_1(l;1) \\ \mathbf{i}_1(l;2) \end{bmatrix} + \begin{bmatrix} \mathbf{H}_{12}(l;1,1) & \mathbf{H}_{12}(l;1,2) \\ \mathbf{H}_{12}(l;2,1) & \mathbf{H}_{12}(l;2,2) \end{bmatrix} \begin{bmatrix} \mathbf{s}_2(l;1) \\ \mathbf{s}_2(l;2) \end{bmatrix}$$

FIG. 20

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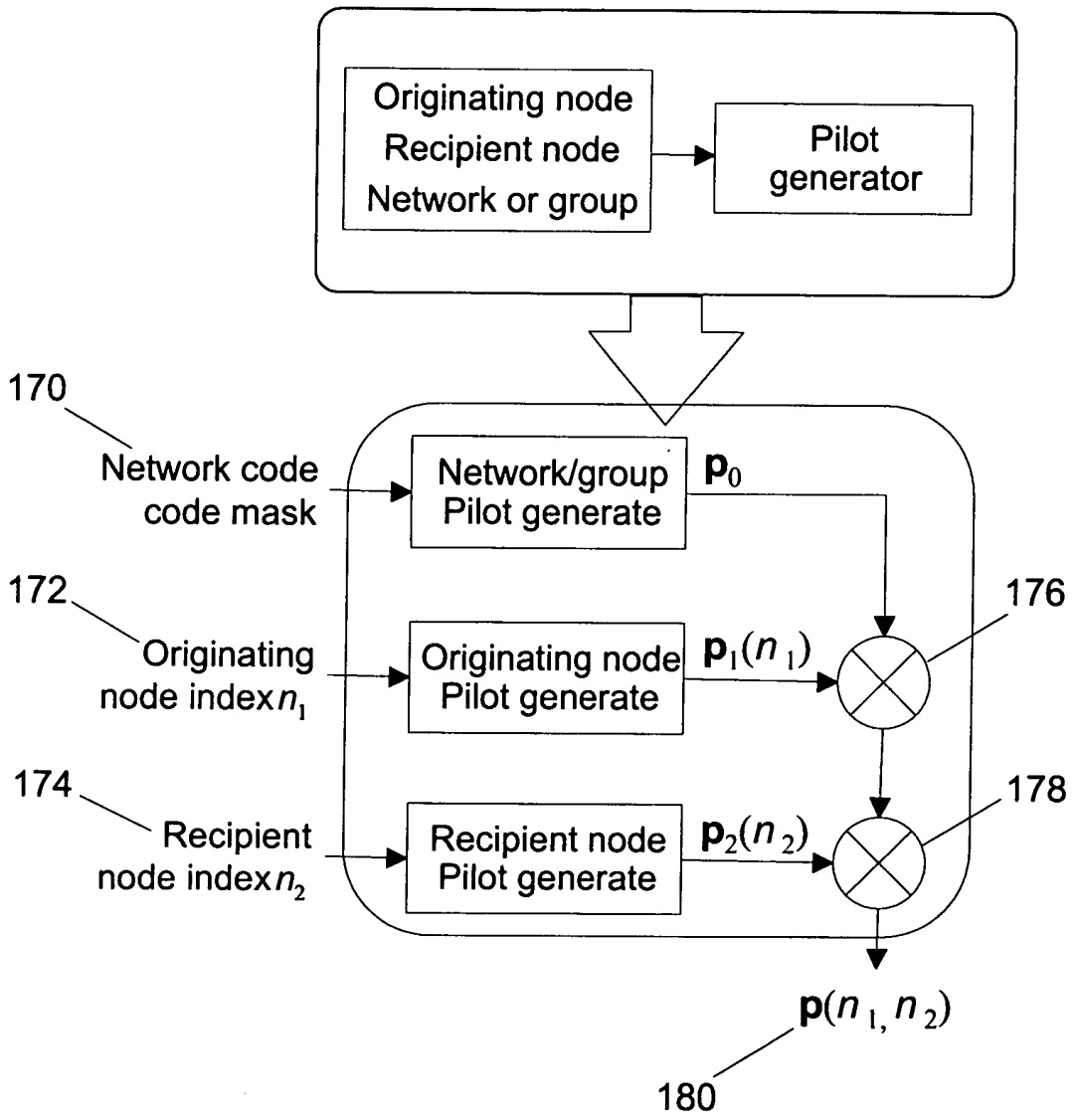

FIG. 21

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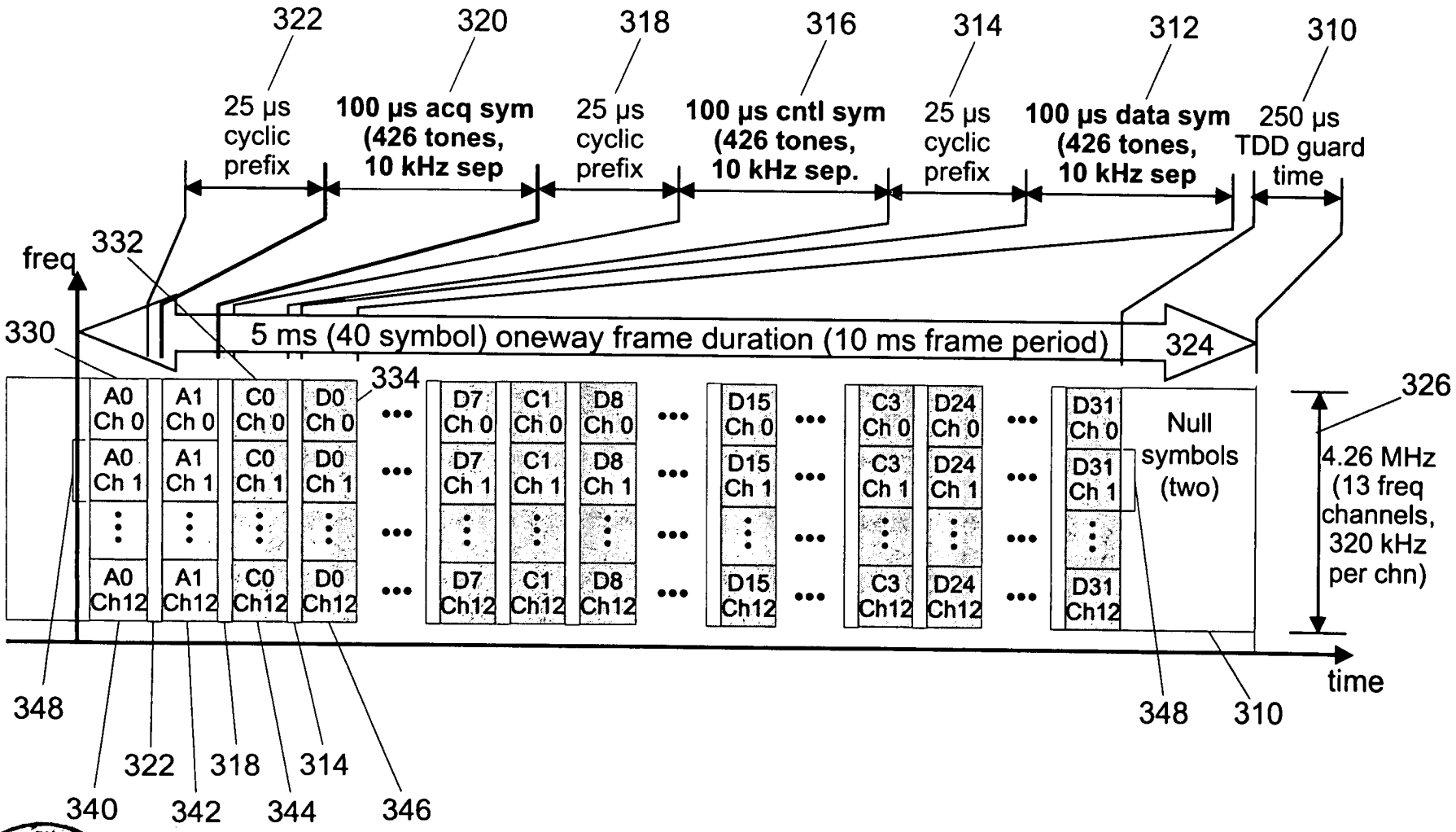

FIG. 22

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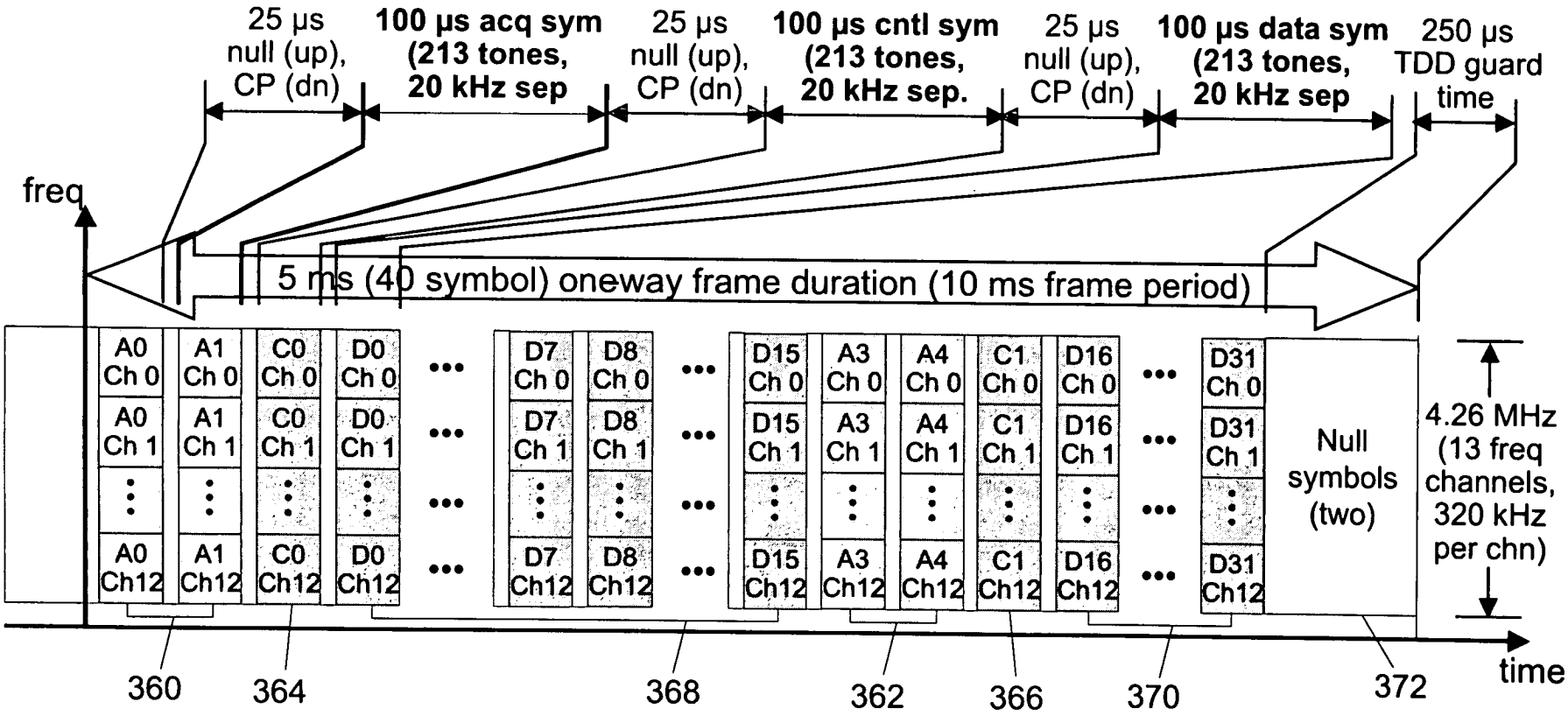

FIG. 23

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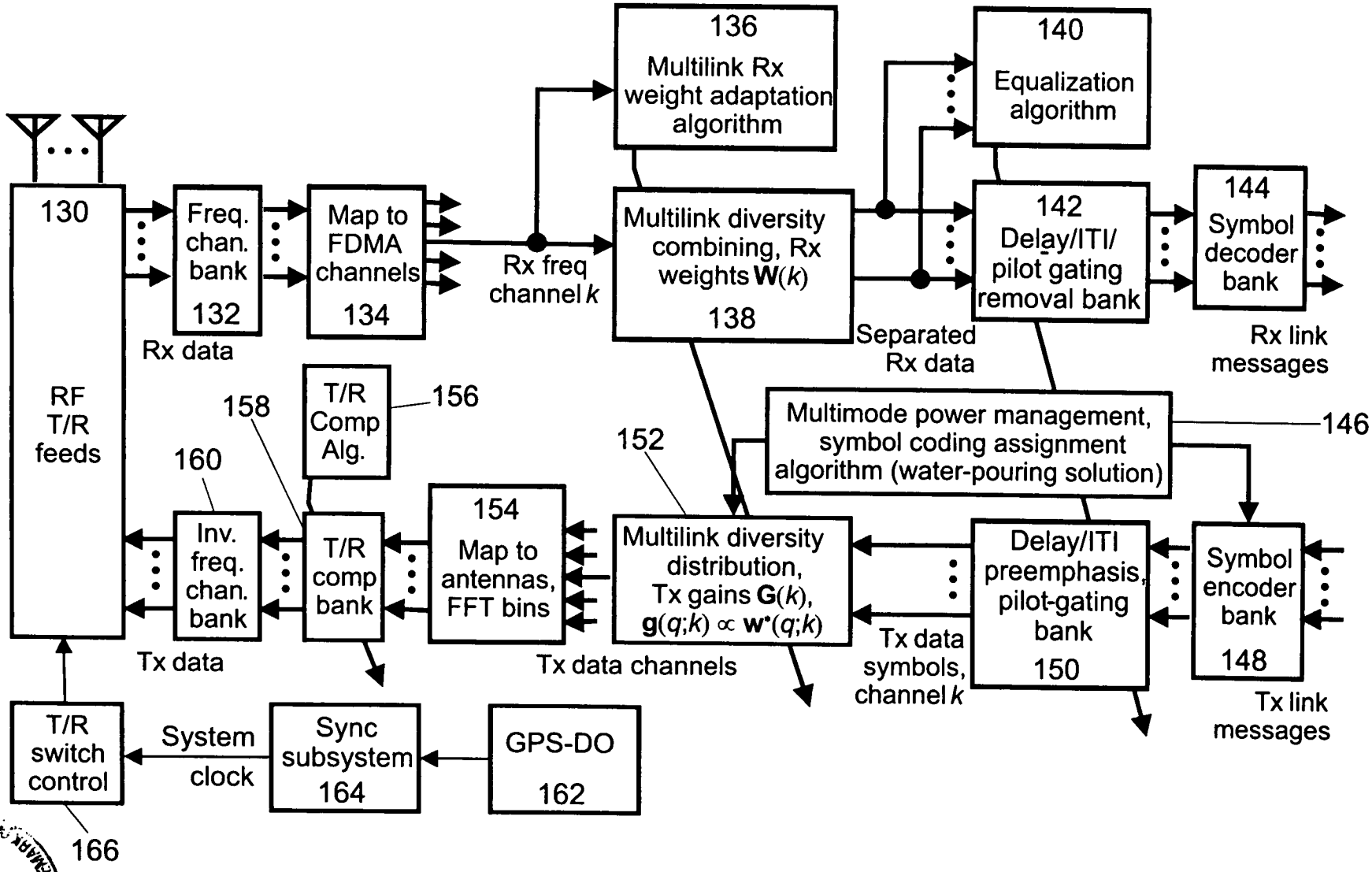

FIG. 24

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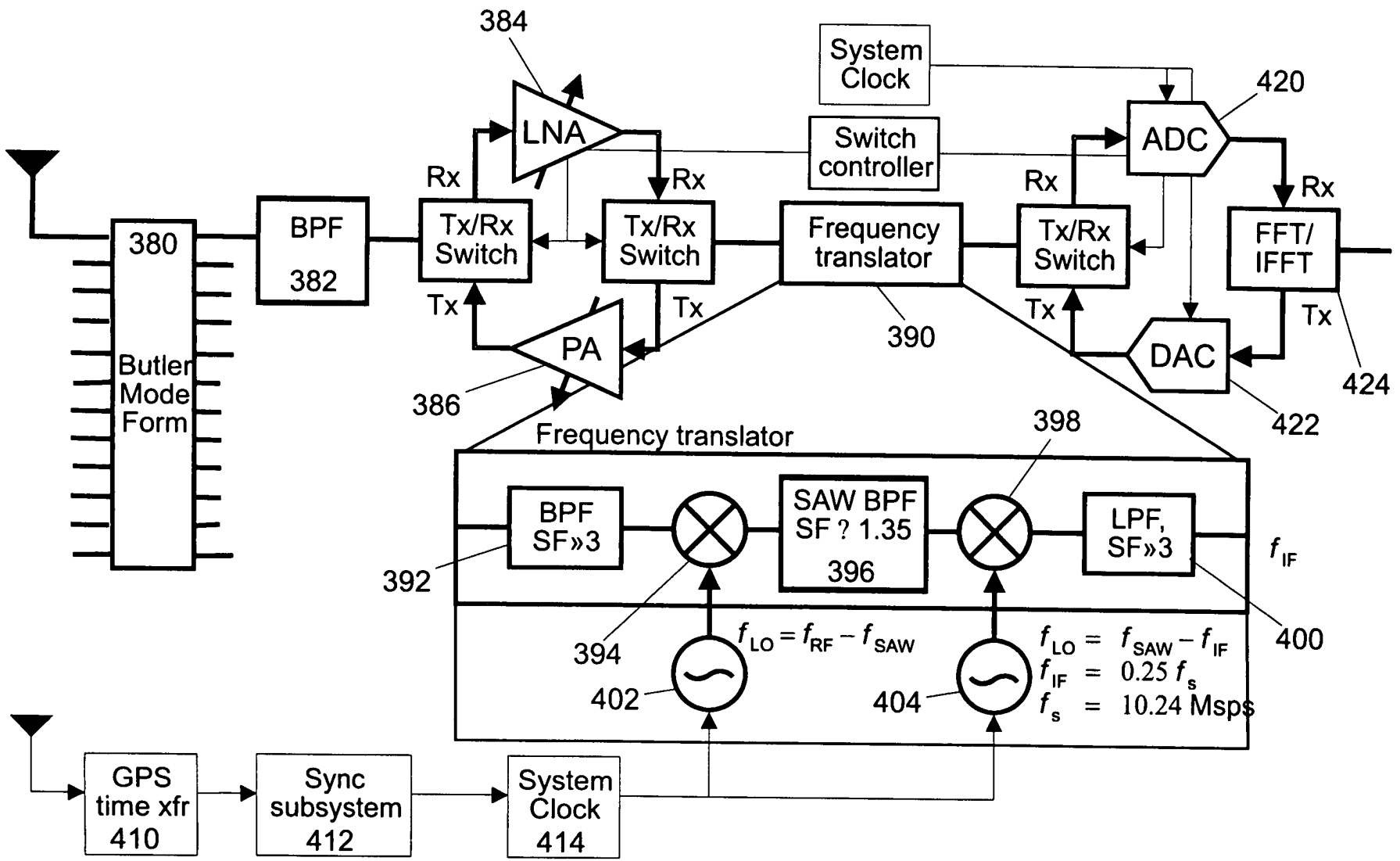

FIG. 25

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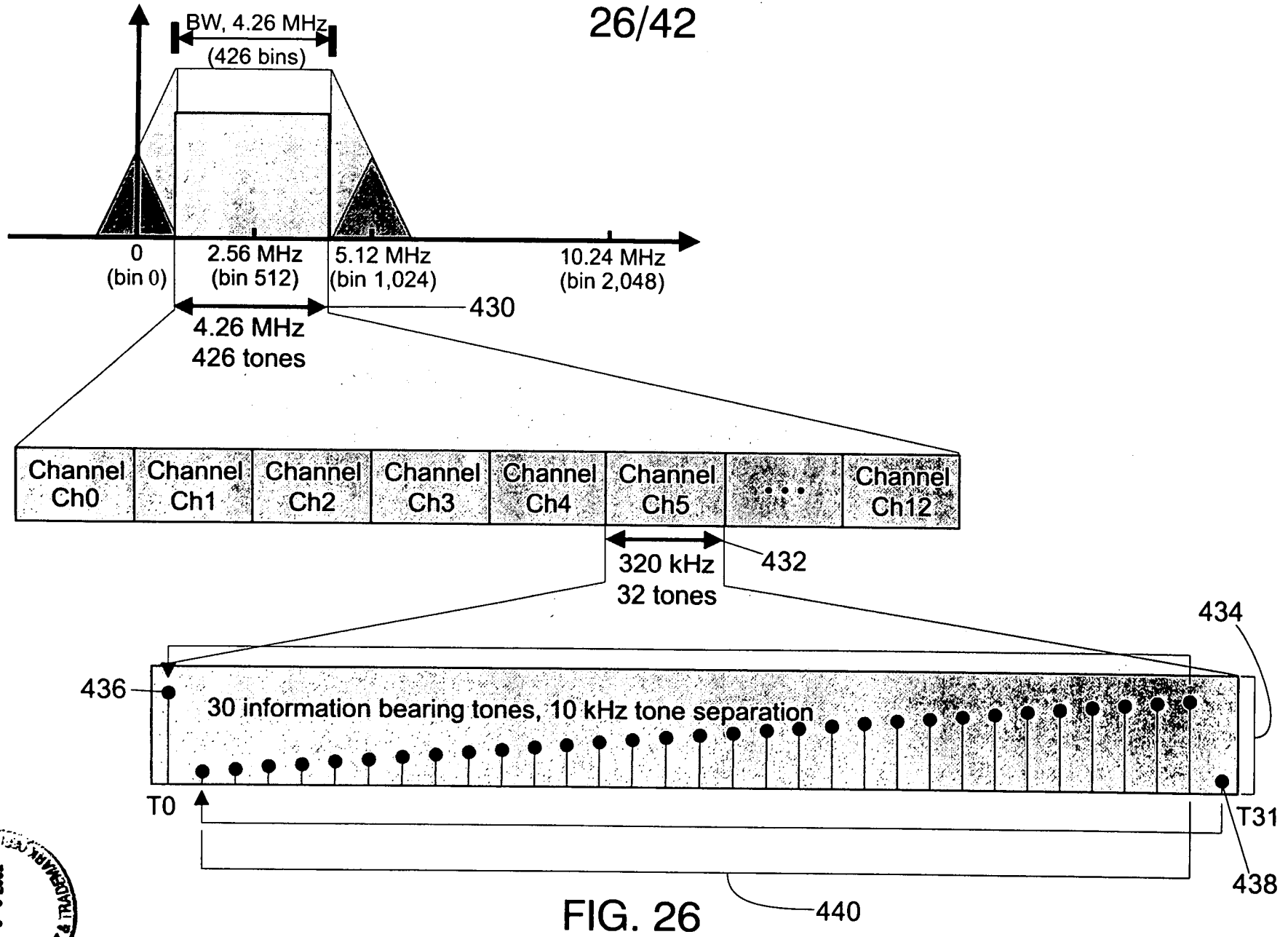

FIG. 26

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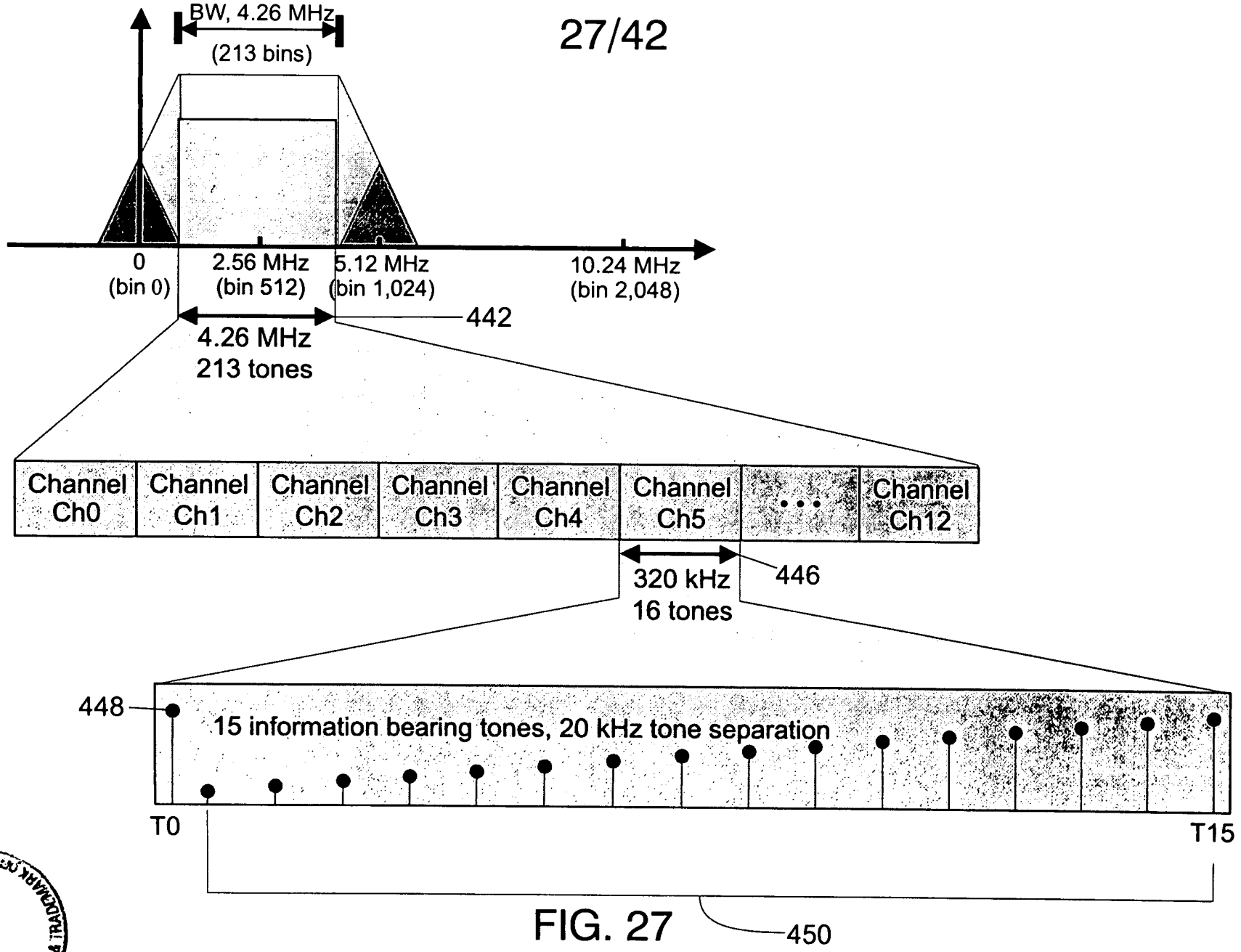

FIG. 27

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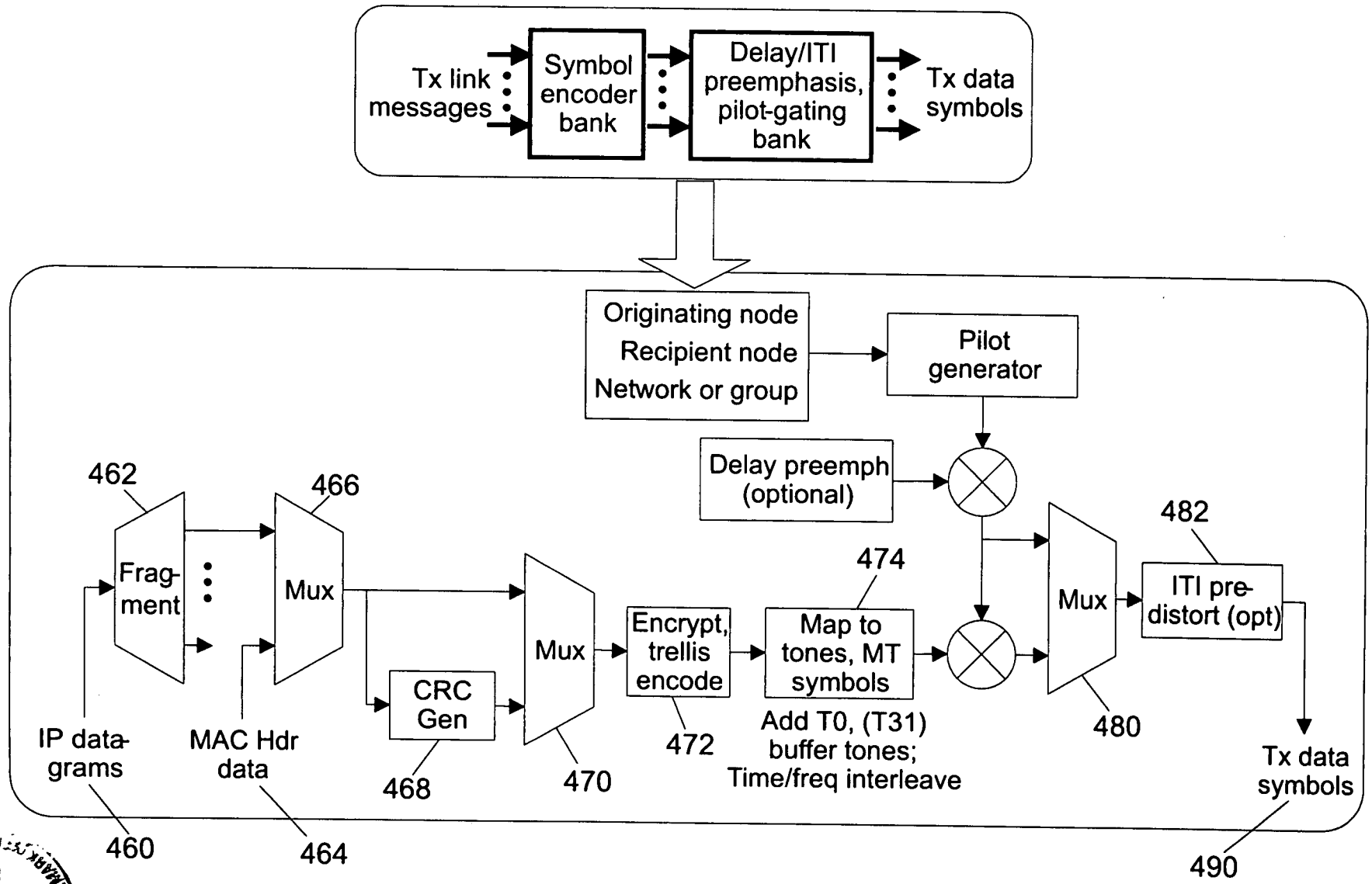

FIG. 28

PTO/SB/21 (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office
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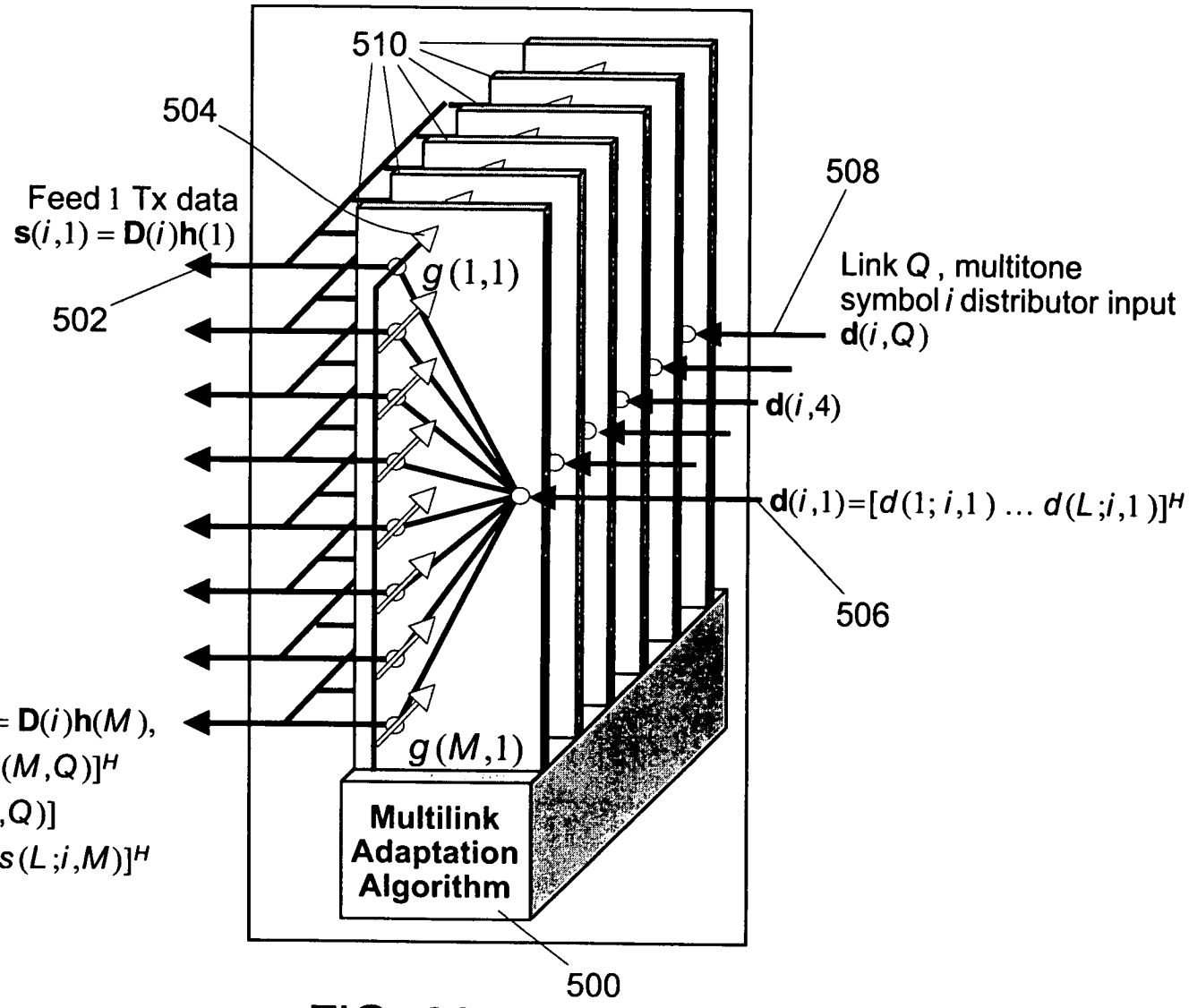

FIG. 29

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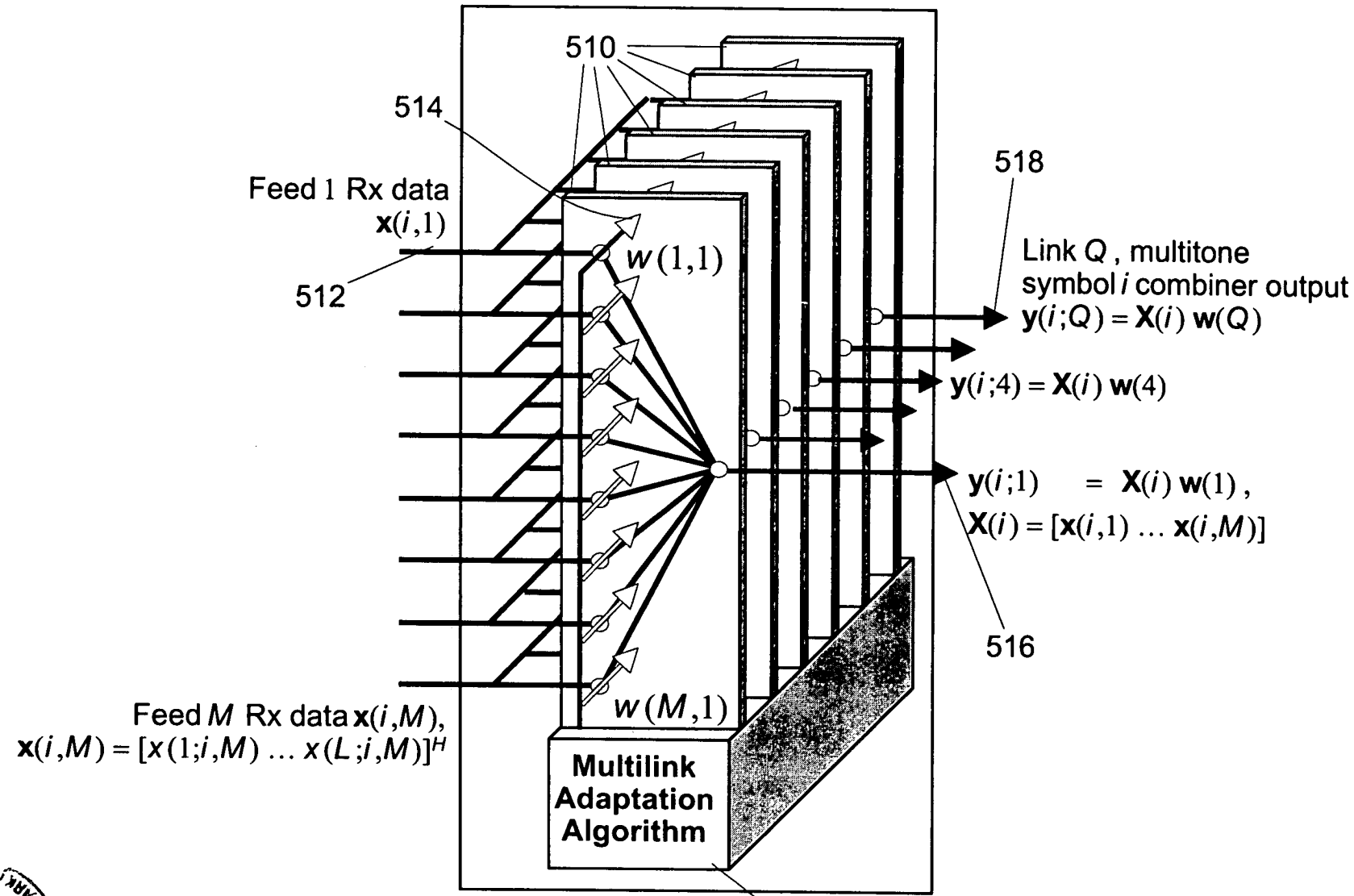

FIG. 30

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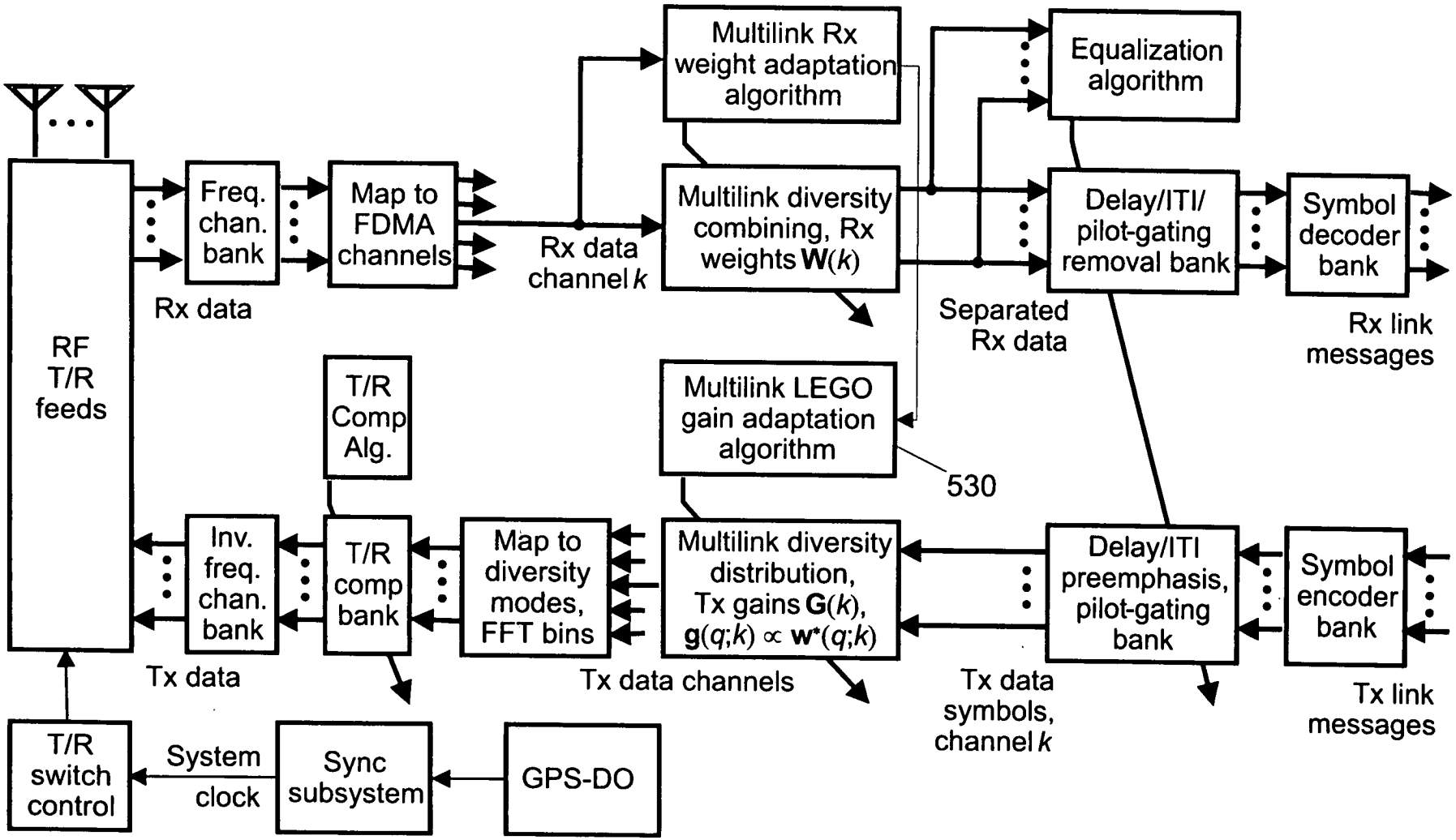

FIG. 31

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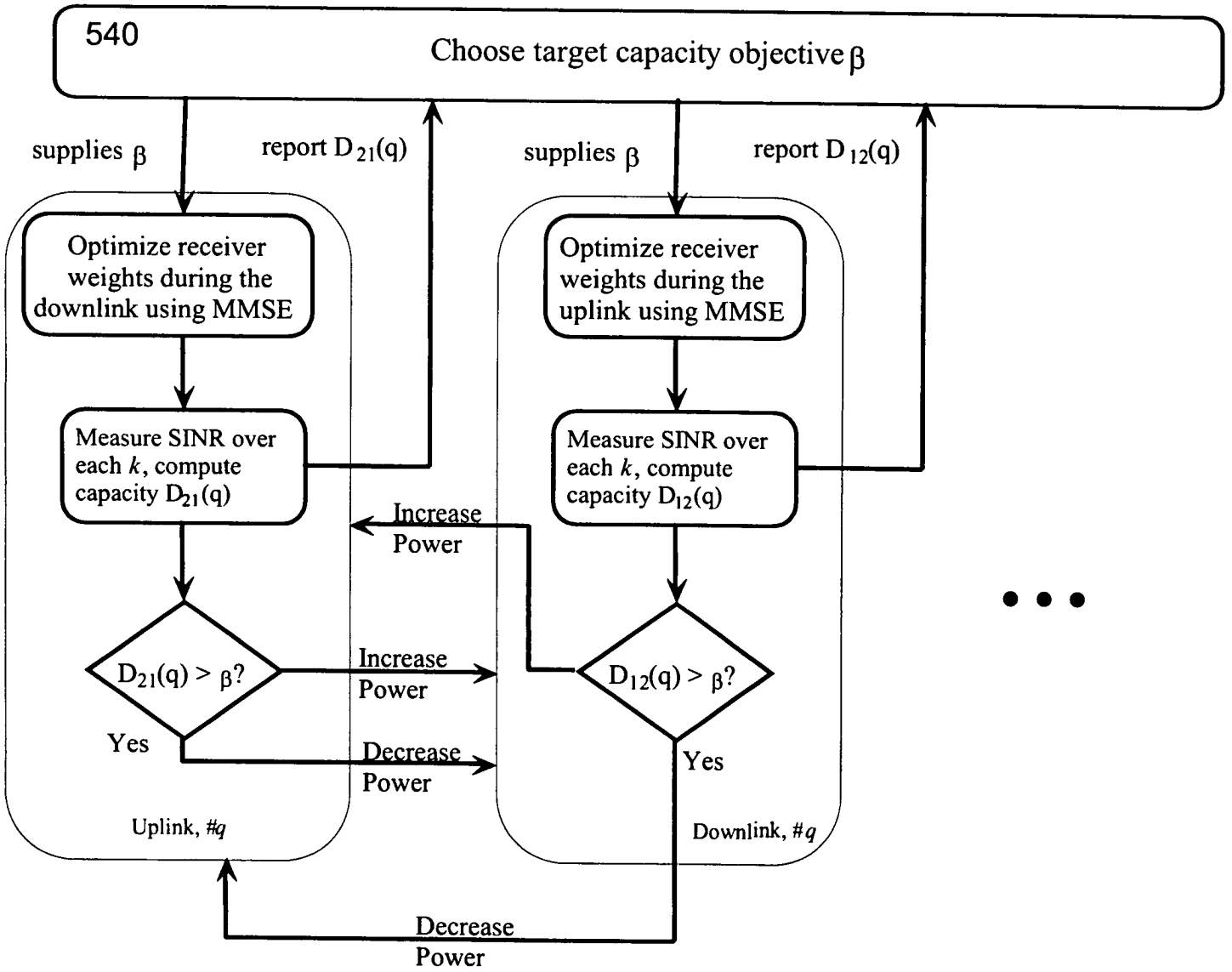

FIG. 32

OIPE OCT 0 8 2002 PATENT & TRADEMARK OFFICE

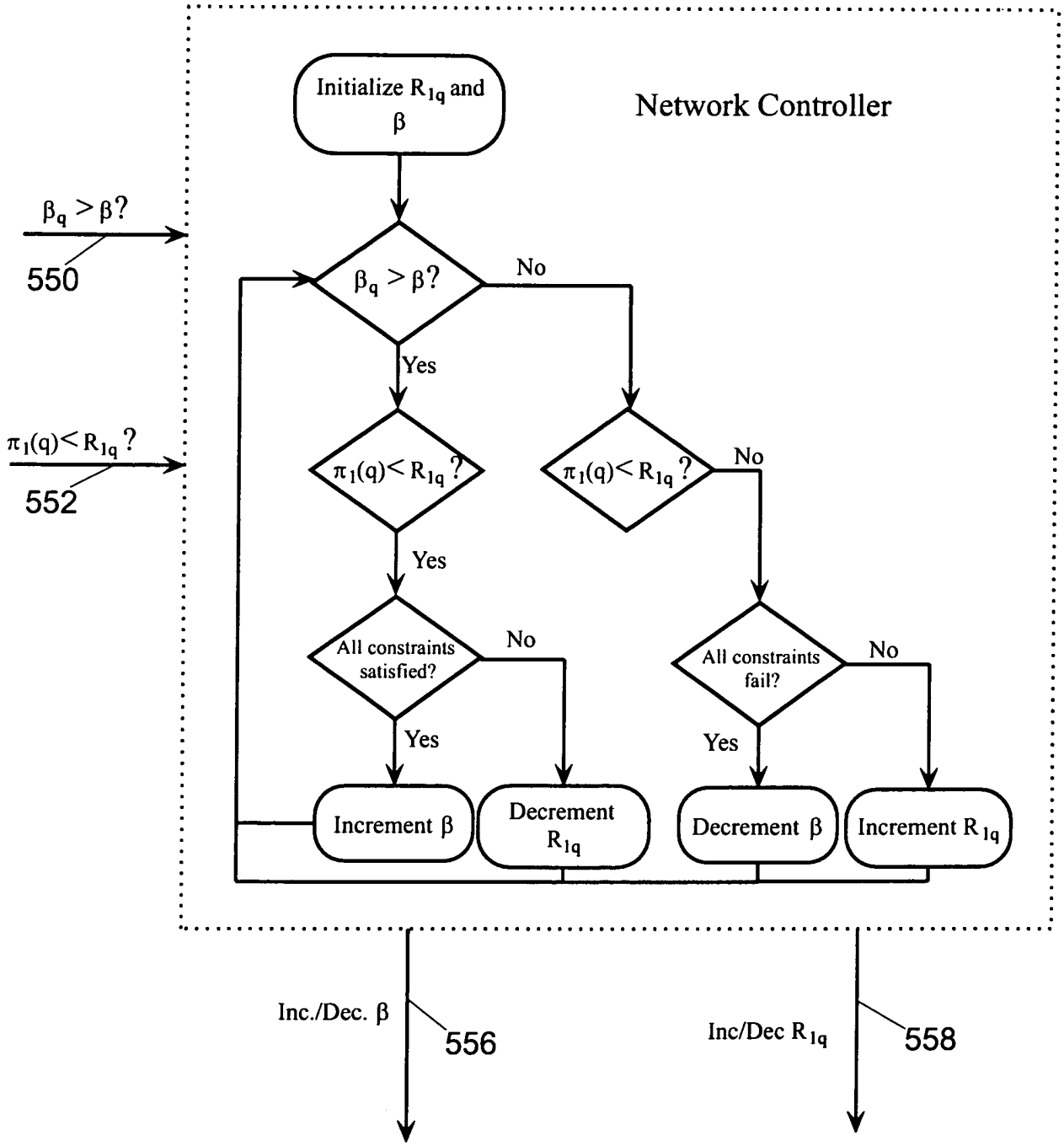

FIG. 33

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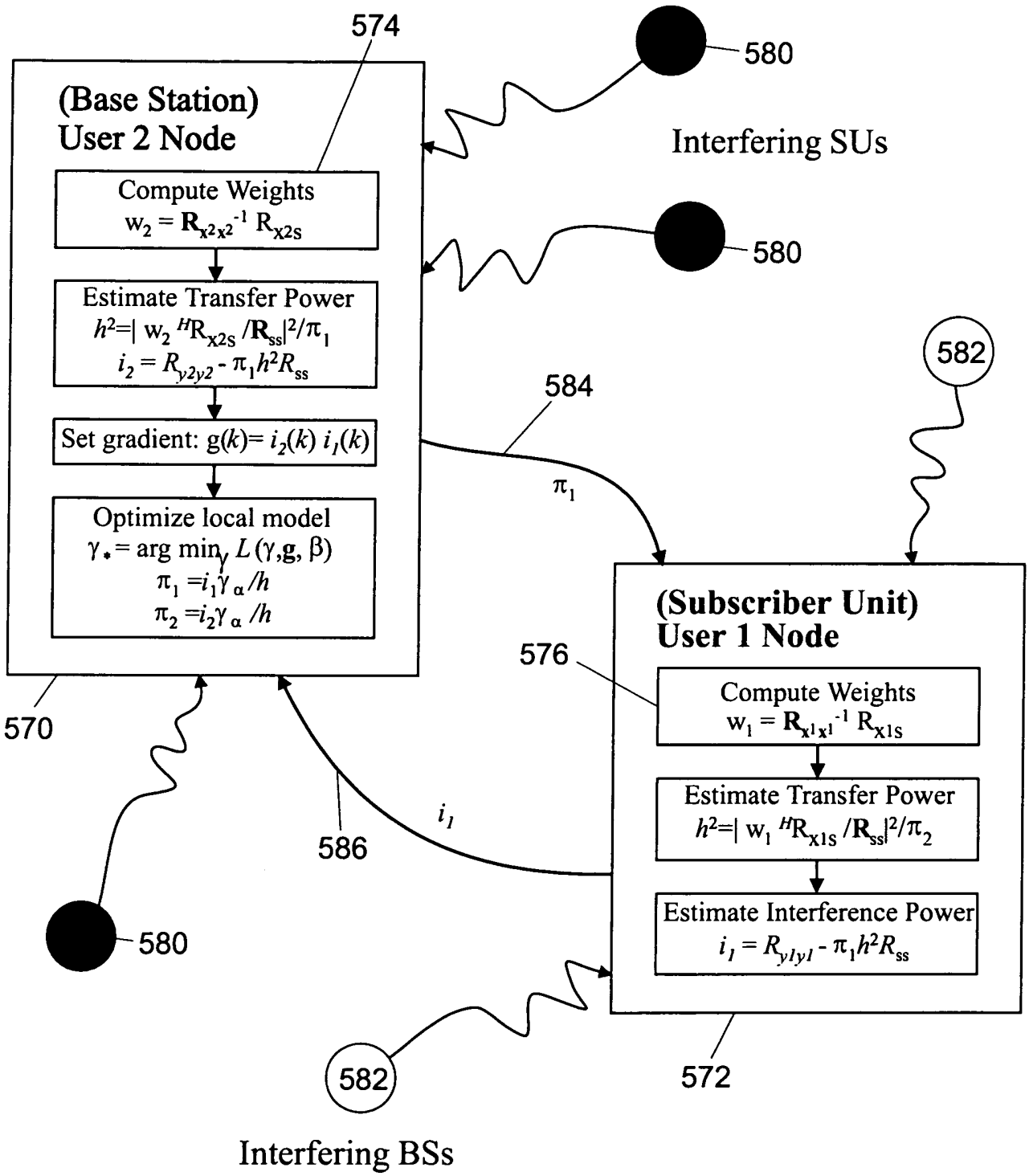

FIG. 34

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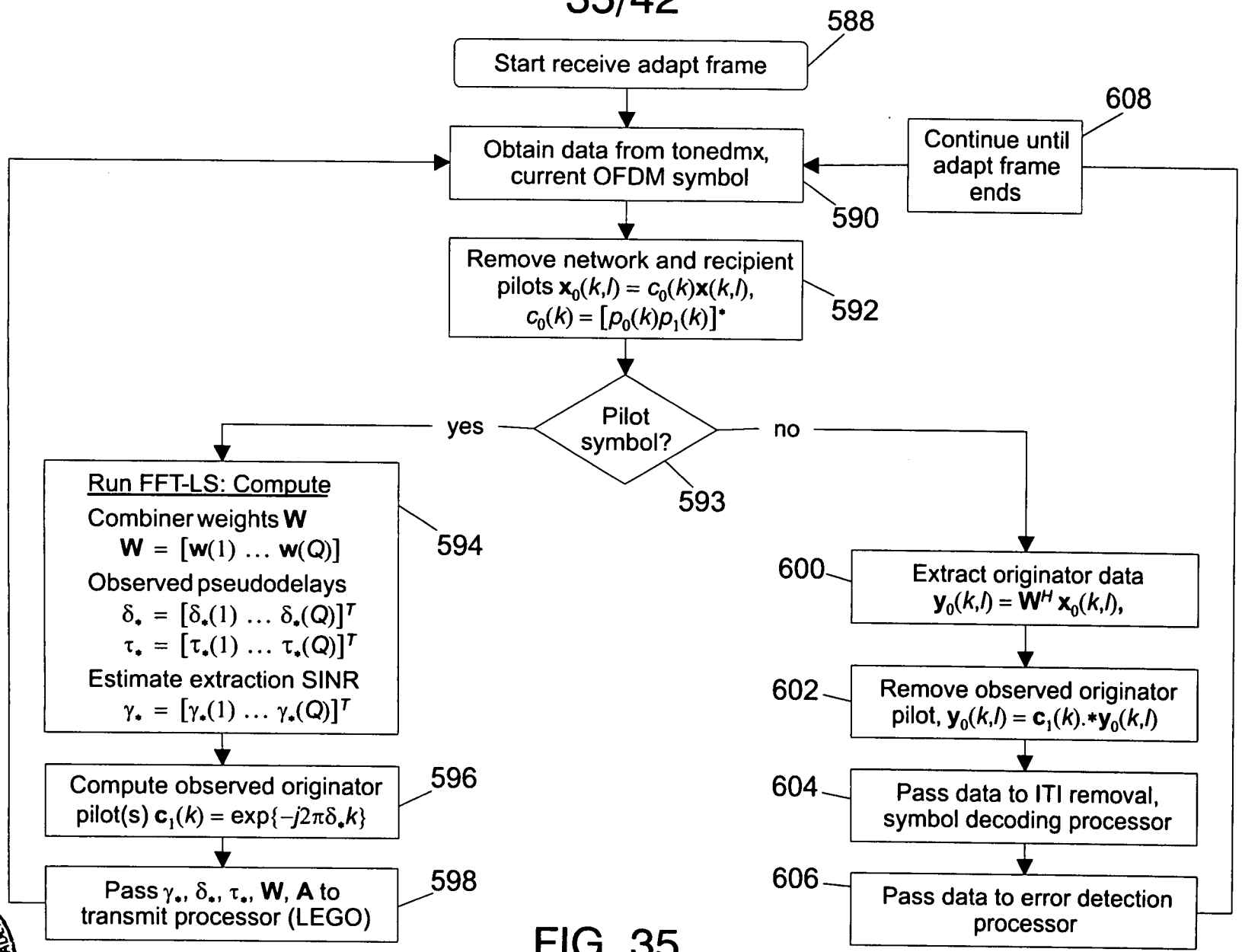

FIG. 35

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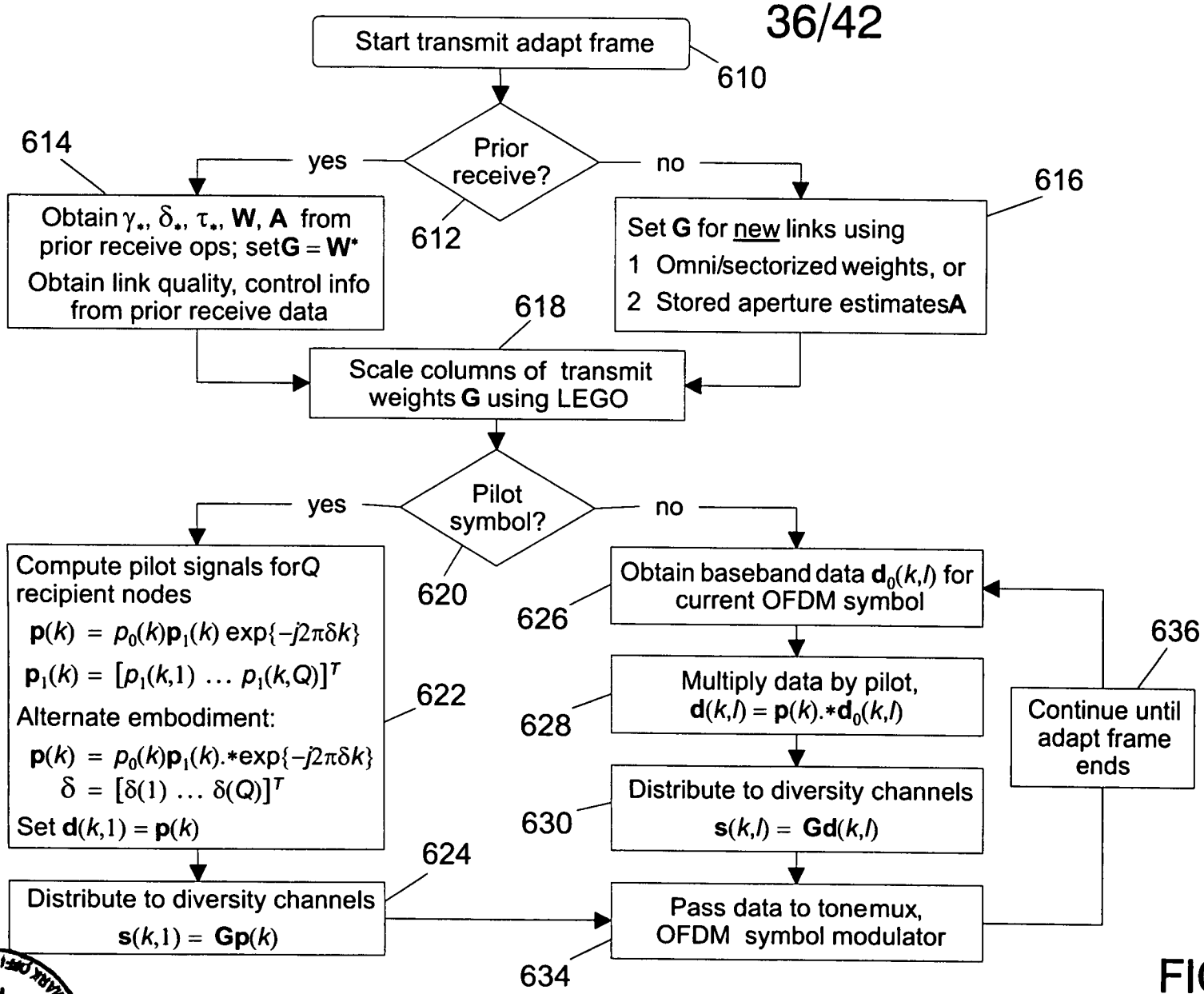

FIG. 36

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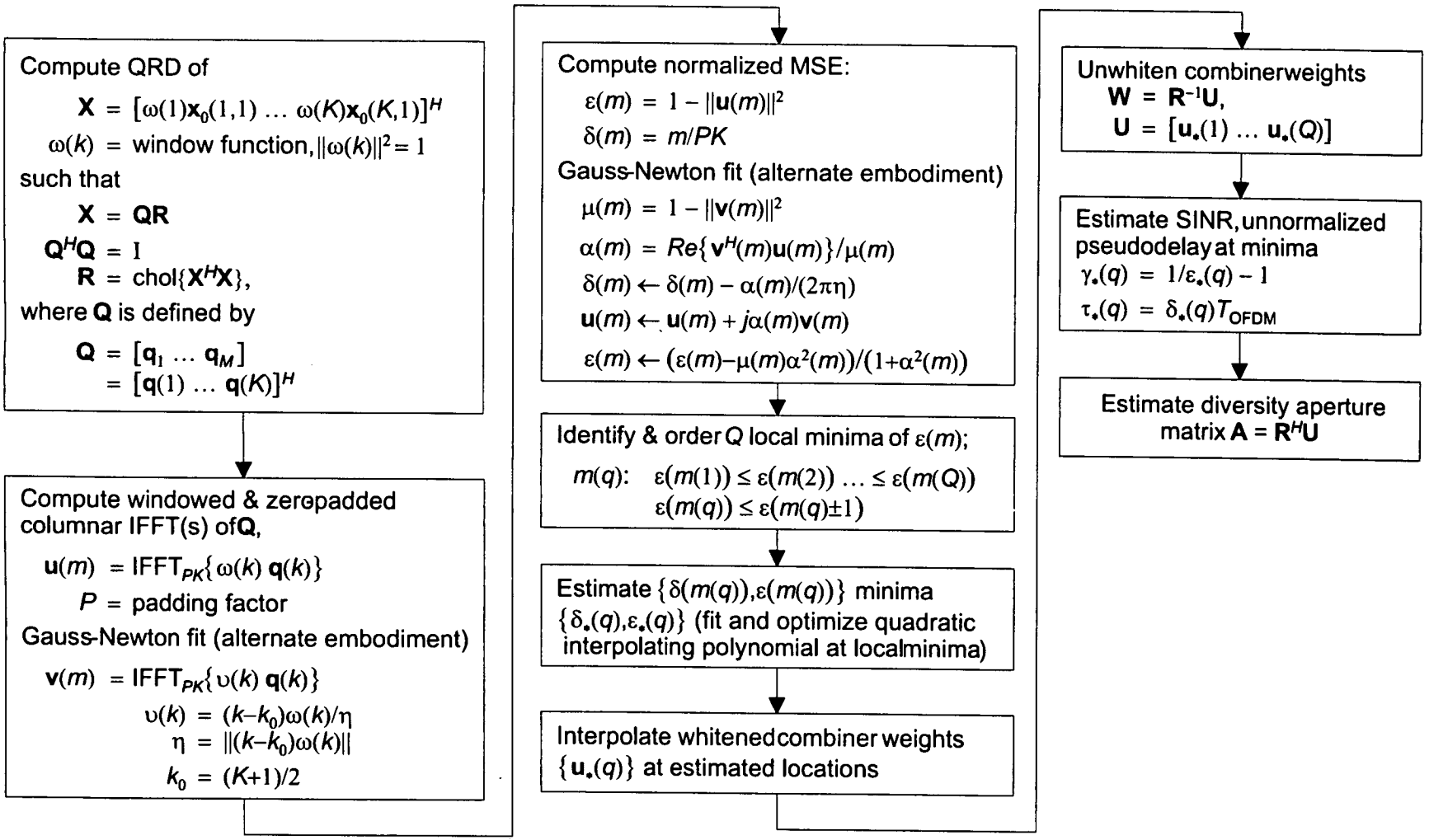

FIG. 37

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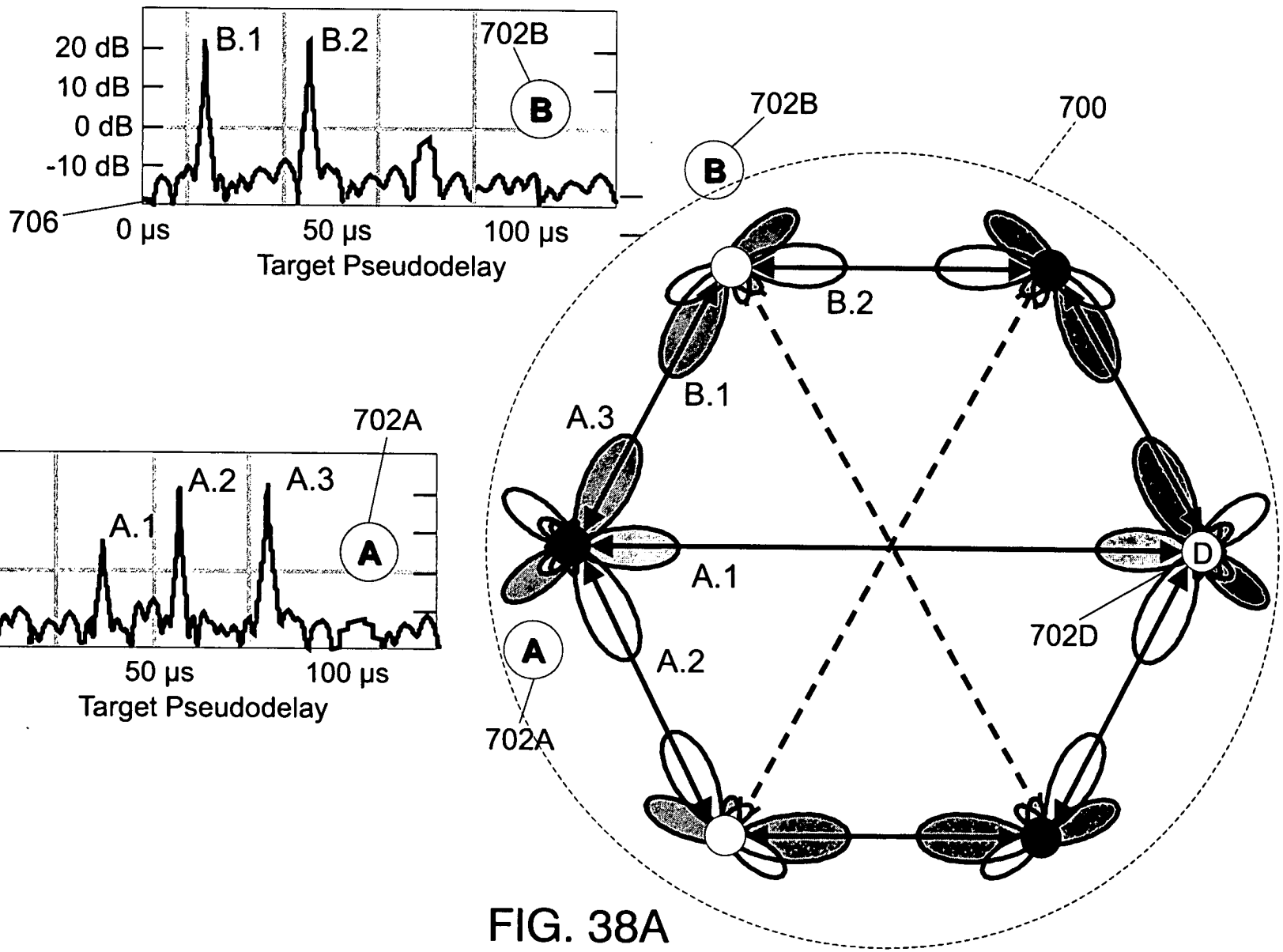

FIG. 38A

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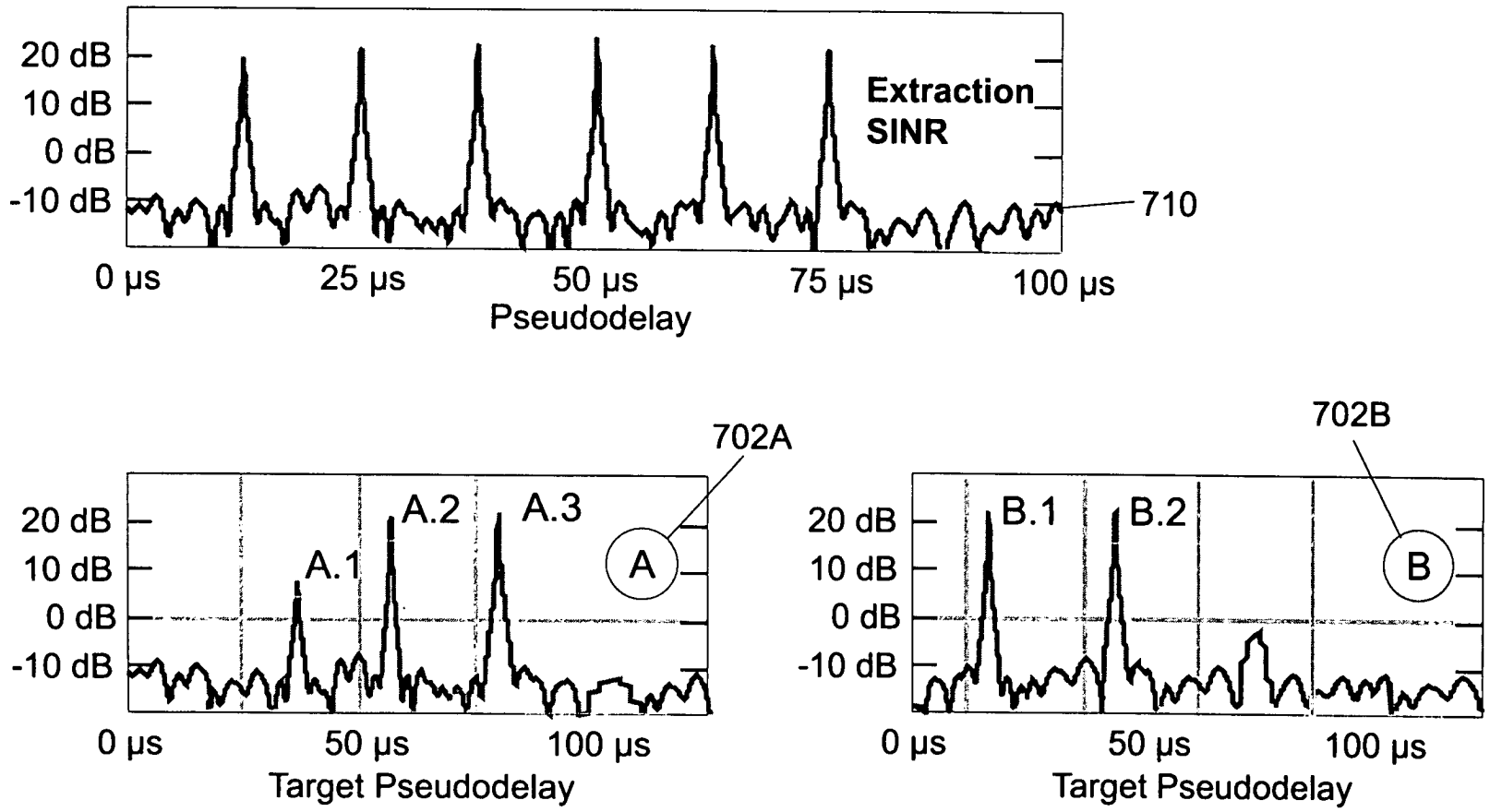

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FIG. 38B

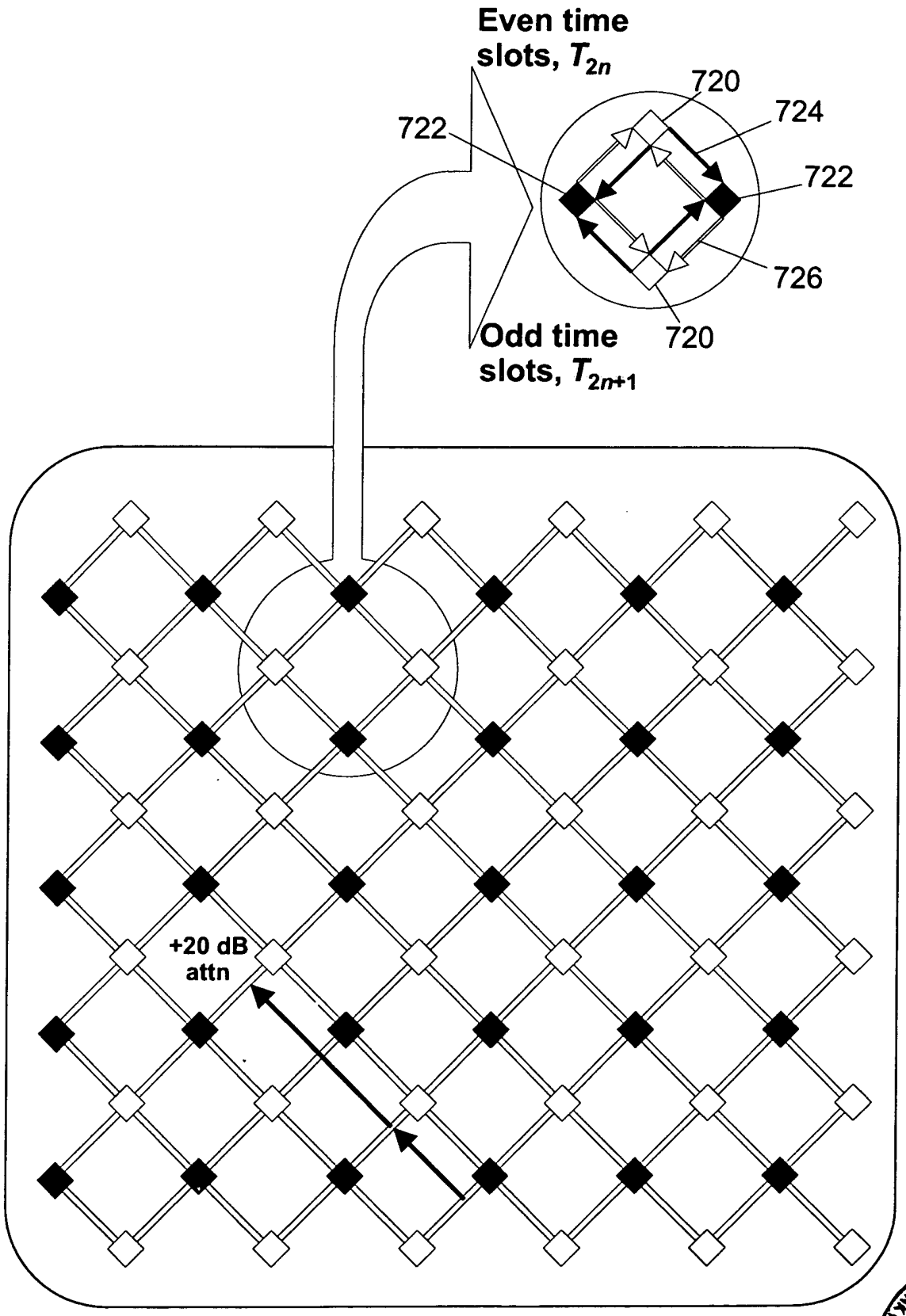

FIG. 39

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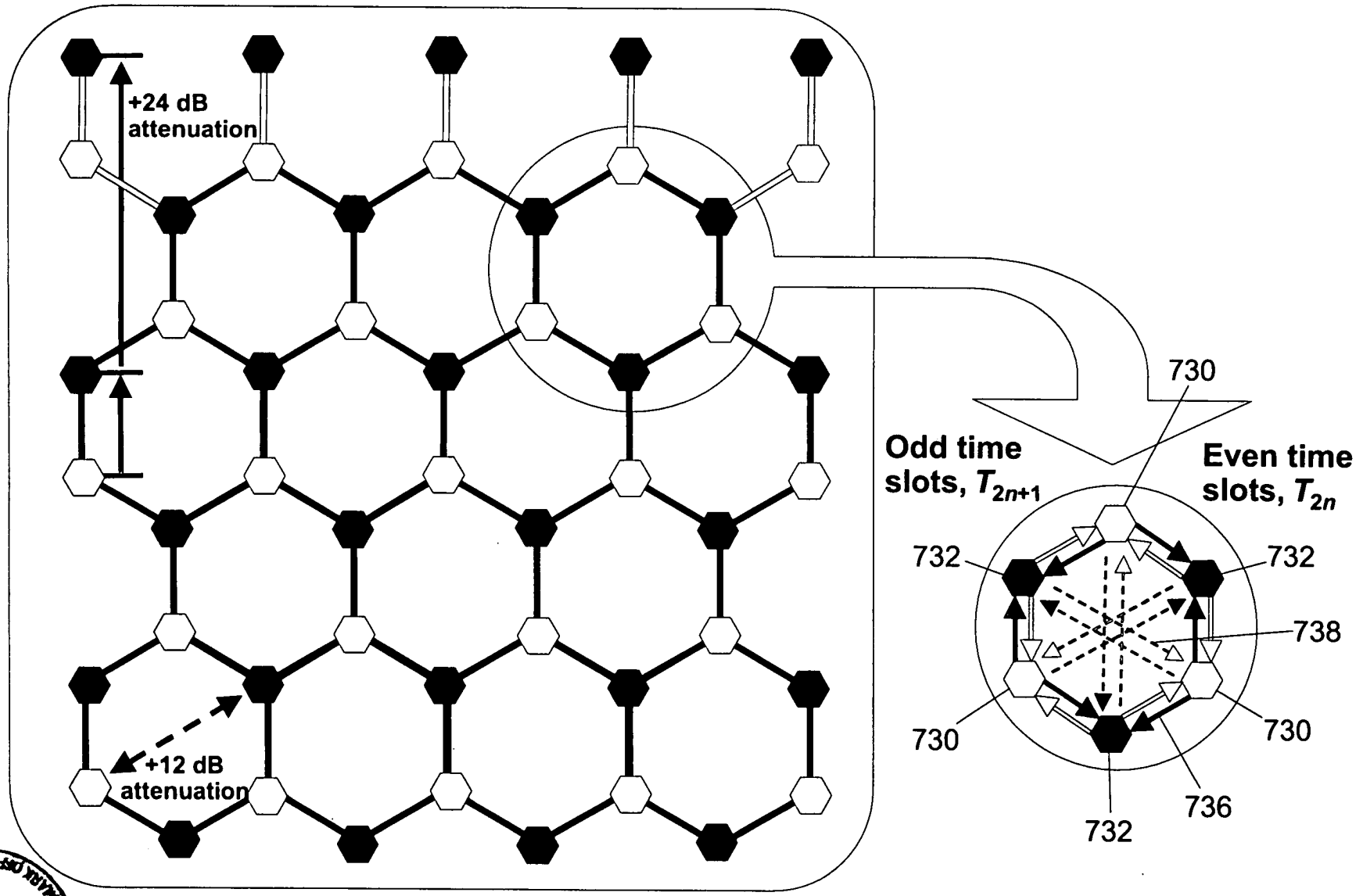

FIG. 40

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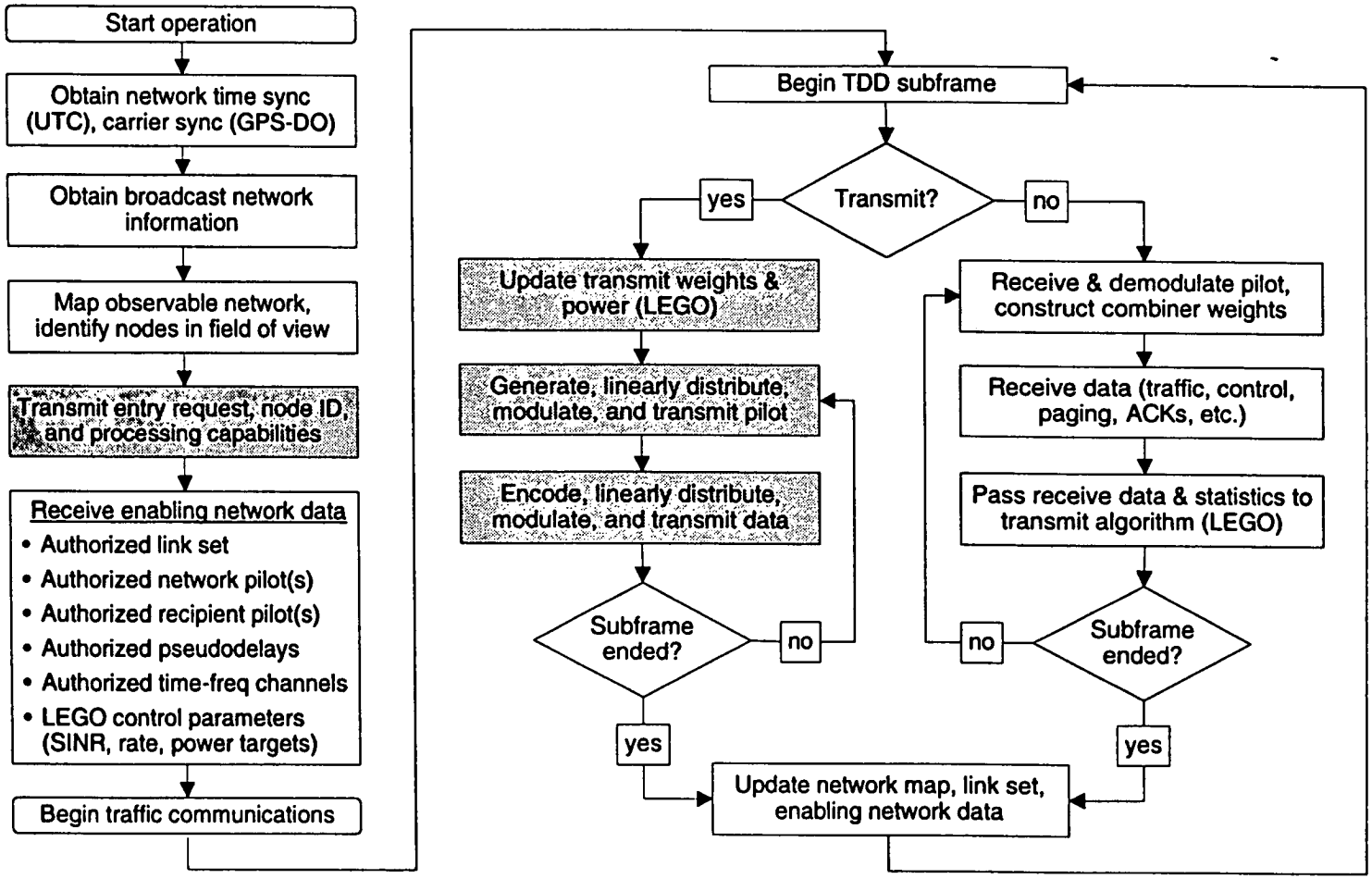

FIG. 41

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